A METHOD OF FORMING AN OPENING OR CAVITY IN A SUBSTRATE FOR RECEIVING AN ELECTRONIC COMPONENT

Background of the Invention

This invention relates to a method of forming an opening or cavity in a substrate. The substrate is preferably of the type which can include an electronic component or integrated circuit. An example of such a substrate is a printed circuit board (PCB).

As circuit density of electronic components, particularly integrated circuits, has increased, there has been a corresponding increase in the problems associated with connecting them to connections and conductors on printed circuit boards (PCB). This problem is particularly severe when there are a large number of interconnects, (for example in the case of micro-processor devices).

Prior Art

Known soldering and wire bonding techniques are expensive and require cumbersome equipment in order to achieve efficiency in the fabrication process. Additionally there may be a requirement to heat the solder twice; firstly on preparation of the PCB and again when mounting components on the PCB

The technique of forming an opening in a substrate for an electronic component is well known, see for example US 3,480,836, which discloses pre-punching holes in a substrate, after which conductor leads having tabs which project over the cavity are attached. This technique has been further developed, for example in US 4,927,491 in which the substrate is a flexible tape.

JP 10098081 discloses using a carbon gas laser to cut a perimeter trench for an opening in a substrate having a copper foil laminated on both sides, the remaining substrate material being removed in a second step. The copper foil is then patterned by lithography and etching to form leads to retain a component.

Summary of the Invention

The present invention arose in order to provide smaller interconnect dimensions on a PCB, thereby rendering it capable of being produced thinner and eliminating the need for synthetic plastics leaded chip carriers (PLCCs). The present invention can also be used to manufacture chip carriers with beneficial properties and lower cost.

According to a first aspect of the present invention there is provided a method as specified in claims 1 - 8. According to a second aspect of the invention there is provided a substrate as specified in claim 9. According to a further aspect the invention provides a device as specified in claim 10.

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying schematic Figures in which:

Brief Description of the Drawings

Figure 1 shows a diagrammatic view of an embodiment of an apparatus for forming interconnects on a substrate;

Figures 2a and 2b are diagrammatic sectional and plan views of a single component mounted on the substrate produced using the apparatus of Figure 1;

Figures 3a to 3c are plan views showing examples of interconnects; and

Figure 4 shows a method of forming a contact through a via hole.

Detailed Description of Certain Advantageous Embodiments

Figure 1 is an overall view of an apparatus 10 for forming interconnects on a substrate 12. The apparatus 10 includes a laser 14, focussed through a suitable lens system 16, which in use, reflects off mirror 18. In the present embodiment a CO_2 laser having a power of 50 - 500 Watts and a beam diameter of 480 microns is used. However, higher powers and larger diameters are desirable for increasing throughput. An Excimer laser or YAG laser can be used as an alternative.

So as to be able to fully appreciate the apparatus it is necessary to consider the apparatus in association with other equipment. These include means for

delivering the substrate, such as a flat bed table 24. Means for selectively removing regions from a first layer of material. This may include a photo imager (not shown) and an etch bath (not shown). Means for removing volumes of the substrate may be a laser 14 or an ion beam etching device (not shown) or a plasma etcher (not shown). Means for removing the material from the second surface, may be a modified etch bath capable of etching an electrical conductor. These in conjunction with the apparatus are controlled by a series of micro-processors (not shown).

Power output of the laser 14 is controlled by micro-processor 20. As well as controlling the pulse duration and energy of the laser 14, micro-processor 20 orientates mirror 18 and may also be used to focus the laser 14 via the lens system 16.

A different depth cavity can be formed either by pulsing a larger number of pulses from the energy source or increasing the duration of each pulse. Similarly an array of cavities can be fabricated, the number and size of cavities in the array can be varied to produce different products or accommodate different devices.

Substrate 12, shown in greater detail in Figure 2, is in the form of a laminated sheet or tape. Two layers 21a and 21b of metallic material, such as copper (or aluminium), sandwich a flexible substrate 12 comprises an etchable polymer such as polyethylene (tri-thalmate) (PET). As substrate 12 is flexible it is delivered on rolls or drums 22a. As substrate 12 is flexible, after it has been connected with components the substrate, including components, can be wound onto another roll 22b.

In the present embodiment the thickness of the substrate is 190 microns, although thicknesses between 100 microns and 600 microns have been employed. Ideally if a silicon chip is to be inserted, it will be ground down from the back to give a similar thickness to that of the substrate. Alternatively, a substrate thickness is chosen according to the thickness of the semiconductor chip.

A non-metallic base material such as PET substrate 12 is clad with a metal material on at least one of its surfaces by laminating a sheet of the metal material, using an adhesive bonding agent or by catalysing the base material and plating a layer of metal which coats the base material in uniform thickness.

Substrate 12 may be introduced in a part finished or 'raw' form. If it is raw, the substrate needs to be treated. This is achieved by firstly coating the substrate with a photoresist. This may be applied as a curtain coat by thin uniform spraying, or using other known techniques.

Conductor tracks, interconnects and die bonding sites are then photo-imaged on both surfaces. This is a routine step in printed wiring board processing.

Using the photo image and etch procedure, a circuit pattern is formed on the metal clad surface of the substrate. The circuit pattern has attachment locations 52 which correspond to bond pad dimensions and locations of a semiconductor component (not shown) to be inserted into the cavity defined on the substrate and connected to interconnects.

On the side of the material opposing the circuit pattern, at an area corresponding to the dimensions of the semiconductor component to be mounted, there are located corresponding bonding pads of the circuit pattern.

Once a region from the upper material has been removed, laser ablation removes the underlying polymer layer defining the substrate. Although mention has been made of PET as the polymer used in the substrate, a variety of other materials are suitable for use. For example, liquid crystal polymers (LCPs), polyamide, PEN / polyethylene napa thalmate, poly vinyl chloride and Mylar (Trademark) can be incorporated into or from the substrate. Another suitable material for fabricating chip carriers is Thermount (Trademark) - available from Dupont – a random strand aramid reinforced laminate material, although this material has poor edge profiling properties it is a very easy material to ablate.

Laser ablation occurs at extremely high rates, typically between 300 to 800 pulses per second. Micro-processor 20 varies the rate and duration of pulses from laser 14. This combination permits the vaporisation rate to be controlled and administered for the specific properties of the substrate material. The result is that ablation occurs at a precise X and Y location over a known area to a predetermined depth for a given array of M rows of cavities by N columns of cavities, defined over a specific area.

Events in the production process are modular. The substrate is firstly coated, then photo-imaged. Etching and stripping then occur. Laser ablation of

the opening or cavity is then performed. The next step is plasma and/or wet chemical cleaning using for example a potassium permanganate solution. After this cleaning step, metal is deposited on the mechanical tab structures such (or contacts) just formed. This is achieved by immersion alloy deposition from solution. This is an electrodeless process, although electroplating could be used as an alternative. The metal alloy chosen must be compatible with the application or bonding method chosen. Typical materials include tin, gold or silver based materials.

During the laser ablation step, material ablated from the cavity can redeposit on other parts of the substrate. Such deposits are usually removed during the plasma and/or wet cleaning step. However, if the material being ablated is polyimide removal can be difficult. To aid removal, an optional sacrificial layer can be deposited on the substrate surface or surfaces prior to the laser ablation step. The sacrificial layer can be photoresist for example. After ablation this layer can be easily removed by plasma and/or wet cleaning, and any redeposited material is removed at the same time.

The PCBs are then cut to shape and finished. This contouring step can be achieved by CNC routing, die punching, or YAG laser contouring

Electrodes are pre-defined by the etching process. A series of digitated connectors, spaced one from another and arranged to be in register with contacts of the component or die to be inserted into the cavity or die are formed by a metal etch process before laser ablation of the dielectric. As an alternative, the electrodes can be laser etched in the metal layer at the base of the cavity after the dielectric material has been ablated. Alternatively, modifications to a pre-etched pattern in this layer can be made with the laser after the cavity has been formed (for example by removing tabs to free the end of an elongate structure).

The perforated substrate with contacts defined on one surface acts as a shelved recess for receiving electronic components (50). The simplest embodiment is an embodiment with one or two contacts, suitable for receiving, for example, capacitors (Figure 3a). Transistors require a third contact to be formed and a sketch of such is shown in Figure 3b. More complex devices, such as integrated circuits (ICs), Read Only Memory (ROM), Random Access Memory

(RAM) or micro-processors require many contacts (51). An example is shown in Figure 3c.

The elongate metal bond leads or tabs which form the electrical contacts perform a dual function. Firstly, they act as electrical pathways to/from components. Secondly, they retain components at least during the fabrication process, due to their mechanical properties. For example, devices can be compression mounted, where insertion of the device causes the projecting tabs to fold, creating resilient clip structures which keep the device in place. It has been found that silver coated contact tabs are particularly advantageous in this application.

Registration of each etched region, on each surface is crucial. However, it will be appreciated that a certain degree of tolerance is permitted and die locations may be offset so as to provide for a suitable mechanical recess, capable of receiving and holding electrical components.

Components can be bonded to the electrodes projecting adjacent the cavity by for example ultrasonic bonding and/or pressure bonding. Alternatively shrink-wrap films can be adapted to urge a component against the electrodes, or an adhesive tape or tab may be used.

The invention may be used to create an array of cavities. An advantage of this arrangement is that a plurality of devices may be produced on a single substrate.

The substrate may be flexible, and capable of being wound or folded so as to ease transportation by reducing its bulk. For example, either prior to and/or after fabrication, the substrate may be stored on a spool.

Components may be introduced into previously formed cavities by any known technique, such as for example a pick-and-place machine, by air jet (vacuum) or by hand. An arrangement whereby a reduced air pressure is created at one surface is particularly convenient. The pressure difference draws electronic components into each cavity, so that the component (such as a semiconductor chip or die) may be bonded to the substrate.

If the present invention is used to make chip carrier circuitry, individual chip carriers may be die cut, routed, or sawn from a relatively large sheet or tape of the substrate.

A particularly advantageous feature of the invention is that it facilitates a flatter chip carrier profile than is normally achievable. Typically thickness of a chip carrier is fabricated in accordance with the invention is 17 micron greater than the die thickness. However, by using the present invention, because a portion of substrate is removed to accept the component, the resultant carrier profile is thinner than has been previously achievable.

Many different types of electrical and electronic components can be placed into the substrate opening or cavity. These include resistors, capacitors, inductors, transistors, integrated circuits, tuners, wave-guides, piezoelectric devices, coils and/or heat-sinks. Additionally, or alternatively, each opening or cavity may be adapted to receive an electro-optical device, such as a liquid crystal device or a light emitting diode. In this latter case conductive tracks may be defined on a surface, using a transparent material such as Indium Tin Oxide (ITO).

In the above embodiments, the opening formed by laser ablation has extended all the way through the substrate. As an alternative a blank opening or cavity may be fabricated by stopping the ablation before all the substrate is removed. This technique is useful for making cavities in multilayer PCBs.

Multilayer PCBs have prepreg dielectric layers, typically 70 microns thick, interleaved with conductive metal layers. The laser ablation process can be used to remove such material to expose bond pads in a subsurface metal layer. A flip chip die with solder bumps can then be placed on top of the bond pads, so that when the assembly is heated the solder flows and bonds the chip in place. An advantage of this technique is that the subsurface layers of the multilayer PCB can be used for signal input and output to the chip, which shortens the signal conductor length and reduces propagation delays.

In addition to the formation of openings or cavities for mounting semiconductor or other devices, it is also possible to ablate via holes through the PCB at the same time. In a preferred embodiment, shown in Figure 4, an elongate flap or tab of metal (30) is left at the bottom of the via hole (31). This flap or tab is

longer than the depth of the via hole, and can optionally have an end shaped to form a serrated edge (32) or a barb or spike. This flap or tab can be urged into the via by blowing a gas or liquid towards the via, or by pushing using a pin or similar solid tool. The part of the flap or tab projecting though the other side of the via hole can then be crimped to a conductive track at the other side of the PCB, forming a through contact without the usual plating steps. In Figure 4 the serrated edges are shown engaging with a second opening or cavity (33) in the substrate, which can be formed by laser ablation or otherwise. This technique may also be advantageous in conventional PCB manufacture, when openings or cavities for receiving electronic devices are not cut in the substrate.

Although in the above embodiment the laser ablation occurs through a patterned metal layer carried by the substrate, it is possible to use a separate metal sheet with corresponding holes cut therein as a mask positioned adjacent the substrate as an alternative.

In the above examples, the laser ablation step exposed elongate contacts which projected into the resulting cavity. Such elongate metal members need not be electrical contacts, however – they can form mechanical structures such as for example for pressure switches.

The invention has been described by way of examples only and variation may be made to the embodiments described, for example by using equivalents not specifically disclosed.

Finally, the document from which this application claims priority, especially the Figures, is incorporated herein by reference.

CLAIMS

1. A method of making an electronic component interconnecting device having a dielectric substrate (12) laminated with a conductive foil (21a, 21b) on first and second sides, characterized by the steps of:

a) creating an interconnecting conductive circuit on the second side of the laminated dielectric substrate by selectively removing portions of the conductive foil (21b) on the second side of the laminated dielectric substrate (12) to leave remaining an interconnecting conductive circuit projecting in part into the perimeter of a preselected volume of the dielectric substrate material;

b) removing conductive foil from the first side (21a) of the laminated dielectric substrate within the perimeter of the preselected volume to expose the dielectric substrate material within said perimeter;

c) removing the volume of the dielectric substrate material within said perimeter to create a void in the dielectric substrate material without destroying the part of the interconnecting conductive circuit projecting into the perimeter of the void;

d) inserting into the void, an electronic component (50) having a thickness not greater than the preselected thickness of the laminated dielectric substrate and having at least one contact (51) corresponding in position to the part of said interconnecting conductive circuit that projects into the perimeter of the void so that when fully inserted, the contact (51) on the electronic component registers with and contacts said projecting part of the interconnecting conductive circuit; and

e) bonding together the contact (51) on the electronic component and the projecting part of the interconnecting conductive circuit to hold the electronic component in the void of the dielectric substrate material.

2. A method of making an electronic component interconnecting device according to claim 1 characterized in that step c) is carried out by a laser (14).

3. A method of making an electronic component interconnecting device according to claim 2 characterized in that the laminated dielectric substrate (12) is moved past the laser (14).

4. A method of making an electronic component interconnecting device according to any preceding claim characterized in that the thickness of the substrate (12) is less than 200 microns.

5. A method of making an electronic component interconnecting device according to any preceding claim characterized in that step a) creates a plurality of conductive tabs which, after step c) project into the perimeter of the void.

6. A method of making an electronic component interconnecting device according to any preceding claim characterized in that the perimeters of the void and electronic component (50) register.

7. A method of making an electronic component interconnecting device according to any preceding claim characterized in that the projecting part of the interconnecting circuit is used as a pressure switch.

8. A method of making an electronic component interconnection device according to any preceding claim characterized in that the laminated dielectric substrate (12) is flexible.

9. A method according to any preceding claim for making a multilayer PCB characterized in that the conductive foil (21b) on the second side of the substrate (12) becomes an inner layer embedded in the multilayer structure, the method including the steps of inserting a flip chip die into the void to contact the exposed embedded conductive foil, and bonding the flip chip die thereto.

10. A method of making an electronic component interconnection device according to any preceding claim further characterized in that the flip chip die includes solder bumps to effect bonding.

11. An electronic interconnecting device comprising a laminated dielectric substrate (12) having a first and a second side and being comprised of a polymer material laminated with a conductive foil (21a, 21b) on both the first and second sides, characterized in that:

a) a circuit is formed in the foil (21b) on the second side of the laminated substrate (12) having at least one interconnecting conductive foil part projecting into the perimeter of a void in the dielectric material at a prescribed location within the perimeter;

b) an electronic component (50) having a thickness not greater than the thickness of the substrate is positioned in the void of the laminated substrate (12) and has at least one contact on its surface that corresponds in position to the said interconnecting conductive foil part and registers with and contacts the at least one interconnecting conductive foil part; and

c) the contact on the component and the at least one interconnecting conductive foil part of the interconnecting device are bonded together to hold the component in the void.

12. An electronic interconnecting device according to any claim 11 characterized in that the thickness of the substrate (12) is less than 200 microns.

13 An electronic interconnecting device according to claim 11 or 12 characterized by a plurality of interconnecting conductive foil parts projecting into the perimeter of the void in the dielectric material at a prescribed locations within the perimeter.

14 An electronic interconnecting device according to claim 11, 12 or 13 characterized in that the perimeter of the electronic component registers with the perimeter of the void.

15. An electronic interconnecting device according to any one of claims 11 to 14 characterized in that the laminated dielectric substrate (12) is one of a tape and sheet.

16. An electronic interconnecting device according to any one of claims 11 to 15 characterized in that the substrate contains a plurality of voids with circuitry formed in the foil associated with each void and within each void is mounted an electronic component.

17. An electronic interconnecting device according to any one of claims 11 to 16 characterized in that the device takes the form of a multilayer PCB and in that the foil on the said second side is a subsurface layer.

18. A method of making an electronic component interconnection device having a dielectric substrate (12) laminated with a conductive foil (21a, 21b) forming electrical conductors on opposite sides of the substrate, and means for connecting these conductors through the thickness of the substrate, characterized by the steps of:

a) selectively removing portions of the conductive foil on one side of the laminated dielectric substrate to leave remaining an elongated interconnecting tab (30) having a free end and being longer than the thickness of the substrate, the free end of the tab projecting into the perimeter of a preselected volume of the dielectric substrate material;

b) removing conductive foil from the other side of the laminated dielectric substrate within the perimeter of the preselected volume to expose the dielectric substrate material completely within said perimeter;

c) removing entirely the volume of the dielectric substrate material within said perimeter to create a void in the dielectric substrate material without destroying the elongated interconnecting tab (30) projecting into the perimeter of the void;

d) moving the free end of the tab (30) through the void to the first-mentioned side of the laminated dielectric substrate; and

e) connecting the tab to the conductive foil on the first-mentioned side of the laminated dielectric substrate.

19. A method of making an electronic component interconnection device according to claim 18 characterized in that step c) is carried out by a laser (14).

20. A method of making an electronic component interconnection device according to claim 18 or 19 characterized in that the laminated dielectric substrate (12) is moved past the laser(14).

21. A method of making an electronic component interconnection device according to claim 18 wherein the laser (14) is a CO_2 laser.

22. A method of making an electronic component interconnection device according to claim 20 characterized in that step a) is carried out using artwork.

23. A method of making an electronic component interconnection device according to any one of claims 18 to 22 characterized in that the dielectric material (12) is a polymer.

24. A method of making an electronic component interconnection device according to any preceding claim characterized in that step c) is followed by deposition of one of tin, silver and gold on the tab (30) projecting into the perimeter of the void.

25. A method of making an electronic component interconnection device according to claim 7 characterized in that the deposition covers all exposed portions of the laminated dielectric substrate (12).

26. An electronic interconnecting device comprising a laminated dielectric substrate (12) having a first and a second side and being comprised of a polymer material laminated with a conductive foil (21a, 21b) defining electrical conductors on both the first and second sides, and means for connecting these conductors through the thickness of the substrate, characterized in that:

a) selected portions of the conductive foil on one side of the substrate are removed to leave an elongated conductive tab (30), the tab having a free end and being longer than the thickness of the substrate;

b) a void is created in the substrate; and

c) the free end of the tab (30) passes through the void to the opposite side of the substrate and is connected to the conductive foil on that opposite side.

27. An electronic component interconnection device according to claim 26 characterized in that all exposed portions of the laminated dielectric substrate are coated.