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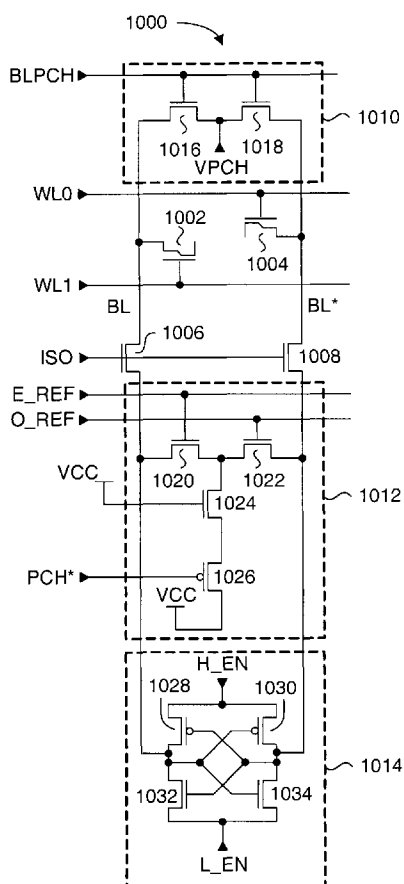
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(54) Title: HIGH SPEED OTP SENSING SCHEME



(57) Abstract: A high speed sensing scheme for a non-volatile memory array is disclosed. The memory array includes non volatile memory cells arranged in a complementary bitline configuration includes precharge circuits for precharging the bitlines to a first voltage level such as VSS, a reference circuits for applying a reference charge on the reference bitlines of the complementary bitline pairs, and bitline sense amplifiers for sensing a voltage differential between the complementary bitline pairs. A voltage on the data bitline being changed when a programmed non-volatile memory cell connected to an activated wordline couples the wordline voltage to the data bitline.

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