Claims

1. A semiconductor die assembly, comprising:

a package substrate including a set of substrate bond pads;

a first semiconductor die attached to the package substrate, the first semiconductor die including a plurality of first die bond pads;

a first support member attached to the package substrate, the first support member located apart from a first edge of the first semiconductor die by a first space, wherein the first support member has a first long axis substantially parallel to the first edge;

a second support member attached to the package substrate, the second support member located apart from a second edge of the first semiconductor die by a second space, wherein the second edge is opposite to the first edge and the second support member has a second long axis substantially parallel to the first long axis;

a third support member attached to the package substrate, the third support member located apart from a third edge of the first semiconductor die by a third space, wherein the third support member has a third long axis substantially perpendicular to the first and second long axes, and wherein the third support member is spaced apart from each of the first and second support members;

a second semiconductor die attached to the first, second, and third support members, wherein a footprint of the second semiconductor die wholly comprises the first semiconductor die, the first support member next to a first border of the footprint, the second support member next to a second border of the footprint, the third support member next to a third border of the footprint, and a fourth space located between a fourth border of the footprint and a fourth edge of the first semiconductor die opposite the third edge;

a die-attach film attaching the first, second, and third support members to the second semiconductor die, but not attaching the first semiconductor die to the second semiconductor die, wherein the die-attach film extends between the second semiconductor die and the first semiconductor die, and between the second semiconductor die and each of the first, second, and third support members; and

a group of wire bonds including: a first subgroup of the wire bonds of the group coupling a first subset of substrate bond pads located in the first, second, and third spaces to corresponding first die bond pads of the plurality; and a second subgroup of the wire bonds of the group coupling a second subset of substrate bond pads located in the fourth space to corresponding first die bond pads of the plurality.

2. The semiconductor die assembly of claim 1, wherein the fourth space includes a first dimension corresponding to a first distance between the first support member and the second support member, and a second dimension corresponding to a second distance between the fourth edge of the first semiconductor die and the fourth border of the footprint, and wherein the second dimension is perpendicular to the first dimension.

3. The semiconductor die assembly of claim 2, wherein the fourth space is exclusive of a support member.

4. The semiconductor die assembly of claim 1, wherein one or more wire bonds of the first subgroup project at least partially into the die-attach film.

5. The semiconductor die assembly of claim 1, wherein one or more wire bonds of the second subgroup project at least partially into the die-attach film.

6. The semiconductor die assembly of claim 1, further comprising:

a package casing that includes an encapsulant at least partially extending into a cavity underneath the second semiconductor die, the cavity defined by the first, second, and third support members, the second semiconductor die, and the package substrate.

7. The semiconductor die assembly of claim 6, wherein the encapsulant surrounds one or more wire bonds of the group, and supports the second semiconductor die.

8. The semiconductor die assembly of claim 1, wherein the second semiconductor die corresponds to a memory die configured to provide data storage, and the first semiconductor die corresponds to a controller die configured to provide memory control.

9. The semiconductor die assembly of claim 1, wherein the second semiconductor die corresponds to a NAND die.

10. The semiconductor die assembly of claim 1, further comprising:

a third semiconductor die located above the second semiconductor die, wherein a first edge of the third semiconductor die is offset with respect to a first edge of the second semiconductor die.

11. The semiconductor die assembly of claim 1, wherein each of the first, second, and third support members comprises a first height that is greater than a second height of the first semiconductor die.

12. The semiconductor die assembly of claim 1, wherein the set of substrate bond pads comprises one or more substrate bond pads configured to couple with one or more circuit components including a capacitor, an inductor, a resistor, a diode, or a combination thereof.

13. The semiconductor die assembly of claim 1, wherein each of the first, second, and third support members comprises silicon.

14. The semiconductor die assembly of claim 1, wherein the die-attach film includes a pressure-set film.

15. A semiconductor die assembly, comprising:

a package substrate including a perimeter and a set of substrate bond pads;

a controller die attached to the package substrate, the controller die including a plurality of controller die bond pads;

a first support member attached to the package substrate, the first support member located apart from a first edge of the controller die by a first space, wherein the first support member has a first long axis substantially parallel to the first edge;

a second support member attached to the package substrate, the second support member located apart from a second edge of the controller die by a second space, wherein the second edge is opposite to the first edge and the second support member has a second long axis substantially parallel to the first long axis;

a third support member attached to the package substrate, the third support member located apart from a third edge of the controller die by a third space, wherein the third support member has a third long axis substantially perpendicular to the first and second long axes, and wherein the third support member is spaced apart from each of the first and second support members;

a first memory die attached to the first, second, and third support members, wherein a footprint of the first memory die wholly comprises the controller die, the first support member next to a first border of the footprint, the second support member next to a second border of the footprint, the third support member next to a third border of the footprint, and a fourth space located between a fourth border of the footprint and a fourth edge of the controller die opposite the third edge;

a first die-attach film attaching the first, second, and third support members to the first memory die, but not attaching the logic die to the first memory die, wherein the first die-attach film extends between the first memory die and the controller die and between the first memory die and each of the first, second, and third support members; and a group of wire bonds including:

a first subgroup of the wire bonds of the group coupling a first subset of substrate bond pads located in the first, second, and third spaces to corresponding controller die bond pads of the plurality; and a second subgroup of the wire bonds of the group coupling a second subset of substrate bond pads located in the fourth space to corresponding controller die bond pads of the plurality.

16. The semiconductor die assembly of claim 15, further comprising: a second memory die located above the first memory die, wherein a first edge of the second memory die is offset by a fifth space with respect to a first edge of the first memory die, wherein the fifth space includes one or more memory bond pads of the first memory die.

17. The semiconductor die assembly of claim 16, further comprising: a third subgroup of the wire bonds of the group coupling a third subset of substrate bond

pads to the one or more memory bond pads of the first memory die, wherein the third subset of substrate bond pads is located between the footprint of the first memory die and the perimeter of the package substrate.

18. The semiconductor die assembly of claim 16, wherein the first and second memory dies comprise NAND dies, respectively.

19. The semiconductor die assembly of claim 16, further comprising: a second die-attach film attaching the second memory die to the first memory die.

20. A semiconductor die assembly, comprising:

a package substrate including a perimeter and a set of substrate bond pads;

a controller die attached to the package substrate, the controller die including a plurality of controller die bond pads;

a first support member attached to the package substrate, the first support member located apart from a first edge of the controller die by a first space, wherein the first support member has a first long axis substantially parallel to the first edge;

a second support member attached to the package substrate, the second support member located apart from a second edge of the controller die by a second space, wherein the second edge is opposite to the first edge and the second support member has a second long axis substantially parallel to the first long axis;

a third support member attached to the package substrate, the third support member located apart from a third edge of the controller die by a third space, wherein the third support member has a third long axis substantially perpendicular to the first and second long axes, and wherein the third support member is spaced apart from each of the first and second support members;

a memory die attached to the first, second, and third support members, wherein a footprint of the first memory die wholly comprises the controller die, the first support member next to a first border of the footprint, the second support member next to a second border of the footprint, the third support member next to a third border of the footprint, and a fourth space located between a fourth border of the footprint and a fourth edge of the controller die opposite the third edge, wherein:

the fourth space includes a first dimension corresponding to a first distance between the first support member and the second support member, and a second dimension corresponding to a second distance between the fourth edge of the controller die and the fourth border of the footprint, and wherein the second dimension is perpendicular to the first dimension, and

the fourth space is exclusive of a support member;

a die-attach film attaching the first, second, and third support members to the memory die, but not attaching the logic die to the memory die, wherein the die-attach film extends between the memory die and the controller die and between the memory die and each of the first, second, and third support members; and

a group of wire bonds including:

a first subgroup of the wire bonds of the group coupling a first subset of substrate bond pads located in the first, second, and third spaces to corresponding controller die bond pads of the plurality, wherein one or more wire bonds of the first subgroup project at least partially into the die-attach film; and

a second subgroup of the wire bonds of the group coupling a second subset of substrate bond pads located in the fourth space to corresponding controller die bond pads of the plurality, wherein one or more wire bonds of the second subgroup project at least partially into the die-attach film.