WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an active pattern on a substrate;

a gate structure in an upper portion of the active pattern;

a bit line structure on the active pattern;

a lower spacer structure extending on a lower portion of a sidewall of the bit line structure;

an upper spacer structure extending on an upper portion of the sidewall of the bit line structure;

a contact plug structure on the active pattern adjacent to the bit line structure; and

a capacitor on the contact plug structure,

wherein the lower spacer structure includes a first lower spacer and a second lower spacer sequentially stacked on the lower portion of the sidewall of the bit line structure, the first lower spacer contacts the lower portion of the sidewall of the bit line structure and does not include nitrogen, and the second lower spacer includes a material different from that of the first lower spacer,

wherein a portion of the upper spacer structure contacts the upper portion of the sidewall of the bit line structure and includes a material different from that of the first lower spacer, and

wherein the first lower spacer and the upper spacer structure completely enclose the second lower spacer.

2. The semiconductor device according to claim 1, wherein the first lower spacer includes silicon oxide or silicon oxycarbide.

3. The semiconductor device according to claim 1 or claim 2, wherein the first lower spacer includes oxide, and the second lower spacer includes nitride.

4. The semiconductor device according to any one of claims 1 to 3, wherein the upper spacer structure includes a first upper spacer, a second upper spacer, and a third upper spacer sequentially stacked on the upper portion of the sidewall of the bit line structure, and

wherein the first upper spacer contacts the upper portion of the sidewall of the bit line structure and includes nitride.

5. The semiconductor device according to claim 4, wherein the second upper spacer is an air spacer, and

wherein the third upper spacer includes nitride.

6. The semiconductor device according to claim 1, wherein the bit line structure includes a first conductive pattern, a diffusion barrier, a second conductive pattern and a capping pattern sequentially stacked on the substrate, and

wherein the first conductive pattern includes polysilicon doped with n-type impurities.

7. The semiconductor device according to claim 6, wherein the lower spacer structure extends on a lower portion of a sidewall of the first conductive pattern of the bit line structure.

8. The semiconductor device according to claim 6 or claim 7, wherein the second conductive pattern includes metal, and

wherein a portion of the upper spacer structure contacts the upper portion of the sidewall of the bit line structure and includes nitride.

9. The semiconductor device according to any one of claims 1 to 8, wherein the second lower spacer is spaced apart from the lower portion of the sidewall of the bit line structure.

10. A semiconductor device comprising:

an active pattern on a substrate;

a gate structure in an upper portion of the active pattern;

a bit line structure on the active pattern, the bit line structure including a first conductive pattern, a diffusion barrier, a second conductive pattern and a capping pattern sequentially stacked on the substrate;

a lower spacer structure extending on a portion of a sidewall of the first conductive pattern of the bit line structure;

an upper spacer structure on the lower spacer structure, the upper spacer structure extending on a portion of a sidewall of the bit line structure;

a contact plug structure on the active pattern adjacent to the bit line structure; and

a capacitor on the contact plug structure,

wherein the first conductive pattern includes polysilicon doped with n-type impurities, and the second conductive pattern includes metal,

wherein the lower spacer structure includes a first lower spacer and a second lower spacer sequentially stacked on the portion of the sidewall of the first conductive pattern of the bit line structure, the first lower spacer contacts the portion of the sidewall of the first conductive pattern and includes oxide, and the second lower spacer includes nitride,

wherein the second lower spacer does not contact the portion of the sidewall of the bit line structure, and a portion of the upper spacer structure contacts the portion of the sidewall of the bit line structure and includes nitride, and

wherein the first lower spacer and the upper spacer structure completely enclose the second lower spacer.

11. The semiconductor device according to claim 10, further comprising third and fourth lower spacers sequentially stacked between the first and second lower spacers,

wherein the third lower spacer includes nitride, and the fourth lower spacer includes oxide.

12. The semiconductor device according to claim 10 or claim 11, wherein the upper spacer structure includes a first upper spacer, a second upper spacer, and a third upper spacer sequentially stacked on the sidewall of the bit line structure, and

wherein the first upper spacer contacts the portion of the sidewall of the bit line structure.

13. The semiconductor device according to claim 12, wherein the second upper spacer is an air spacer, and

wherein the third upper spacer includes nitride.

14. The semiconductor device according to any one of claims 10 to 13, wherein the second lower spacer is spaced apart from the sidewall of the first conductive pattern.

15. A semiconductor device comprising:

an active pattern on a substrate;

a gate structure in an upper portion of the active pattern;

a bit line structure on the active pattern, the bit line structure including a first conductive pattern, a second conductive pattern and a capping pattern sequentially stacked on the substrate;

a first spacer on a sidewall of the first conductive pattern, the first spacer including silicon oxide;

a second spacer extending on an outer sidewall of the first spacer and sidewalls of the second conductive pattern and the capping pattern;

a third spacer and a fourth spacer sequentially stacked on a lower portion of an outer sidewall of the second spacer;

a fifth spacer and a sixth spacer sequentially stacked on an upper portion of the outer sidewall of the second spacer;

a contact plug structure on the active pattern adjacent to the bit line structure; and

a capacitor on the contact plug structure,

wherein the third spacer, the fifth spacer, and the sixth spacer completely enclose the fourth spacer.

16. The semiconductor device according to claim 15, wherein the first conductive pattern includes polysilicon doped with n-type impurities, and the second conductive pattern includes metal.

17. The semiconductor device according to claim 15 or claim 16, wherein the second spacer includes nitride.

18. The semiconductor device according to any one of claims 15 to 17, wherein the bit line structure further includes a diffusion barrier between the first and second conductive patterns, and

wherein the second spacer extends on a sidewall of the diffusion barrier.

19. The semiconductor device according to any one of claims 15 to 18, wherein the third spacer includes oxide, and the fourth spacer includes nitride, and

wherein the fifth spacer includes a cavity, and the sixth spacer includes nitride.

20. The semiconductor device according to any one of claims 15 to 19, wherein the second spacer is spaced apart from the sidewall of the first conductive pattern.