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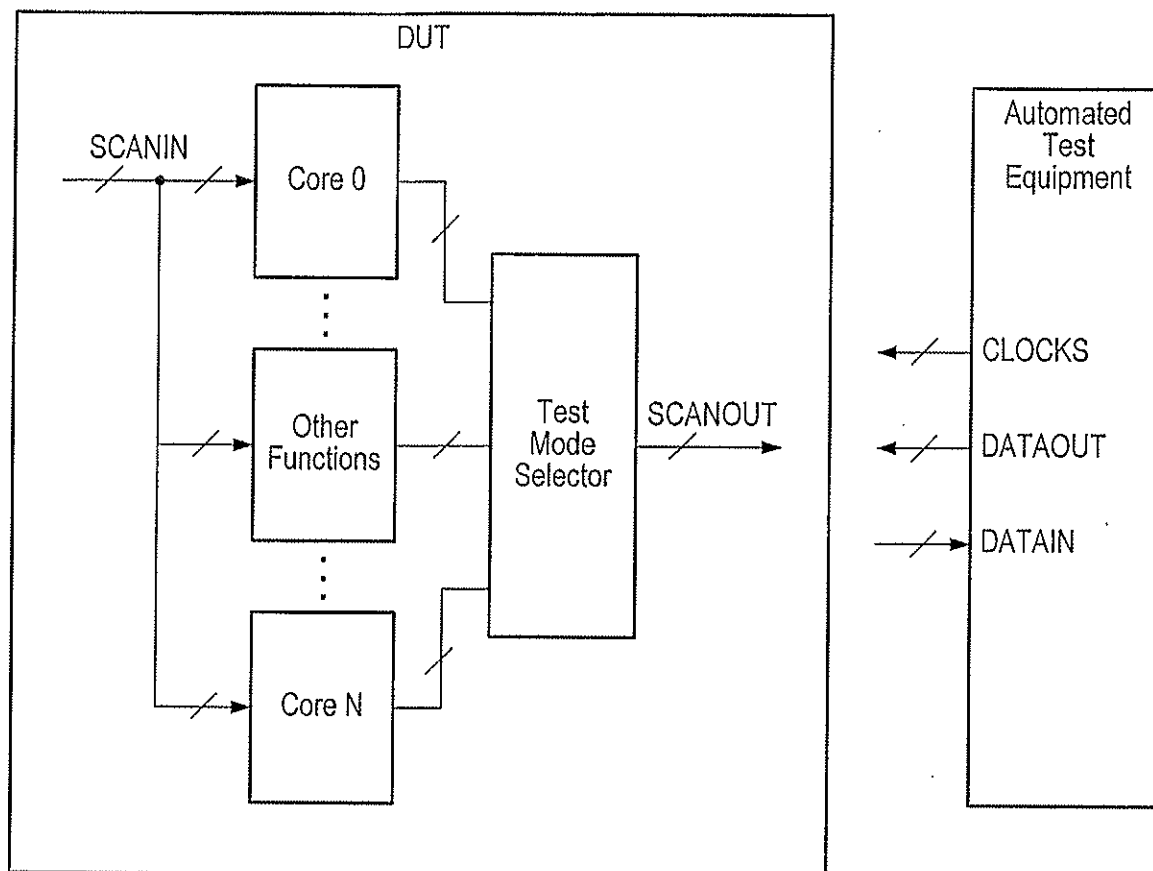


FIG. 1

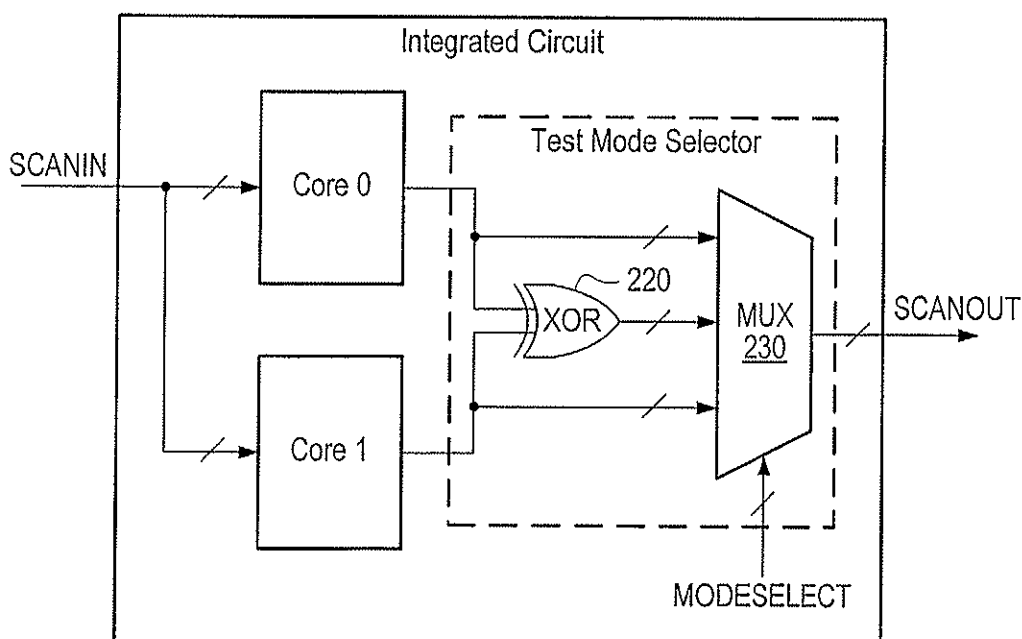


FIG. 2

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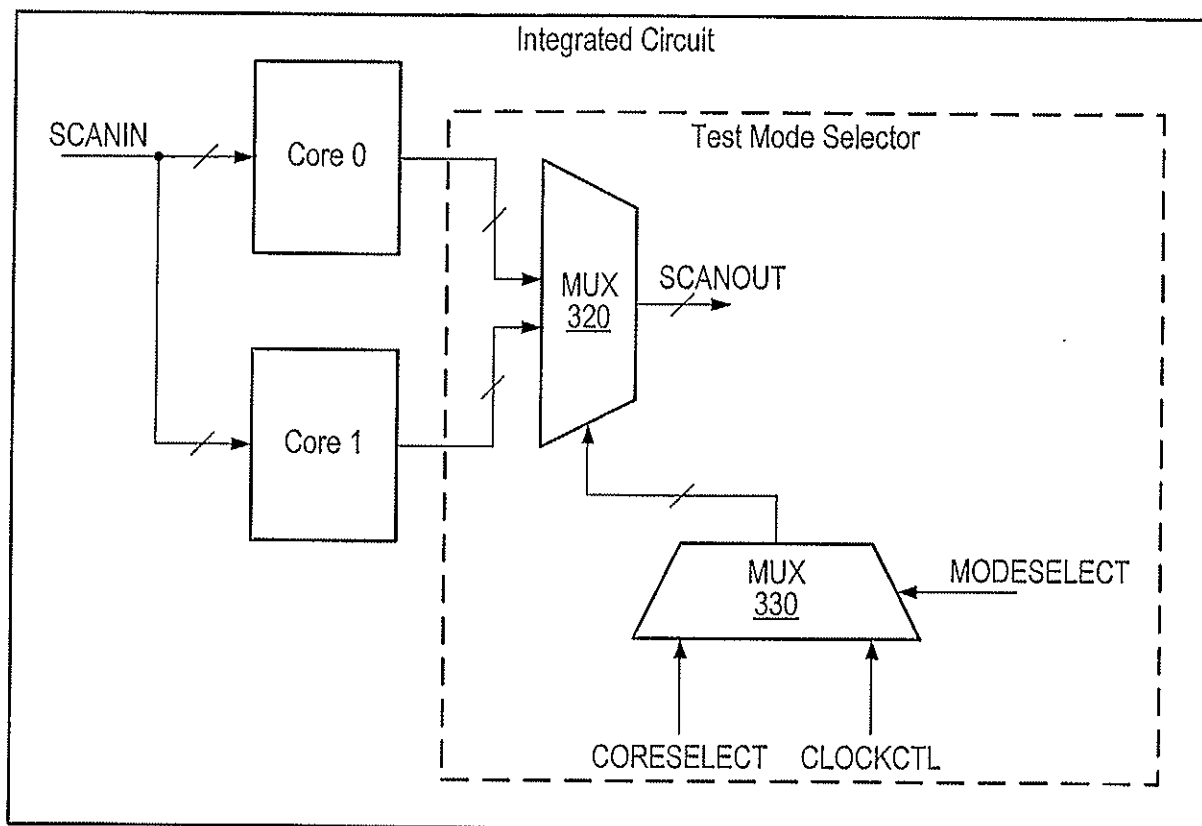


FIG. 3

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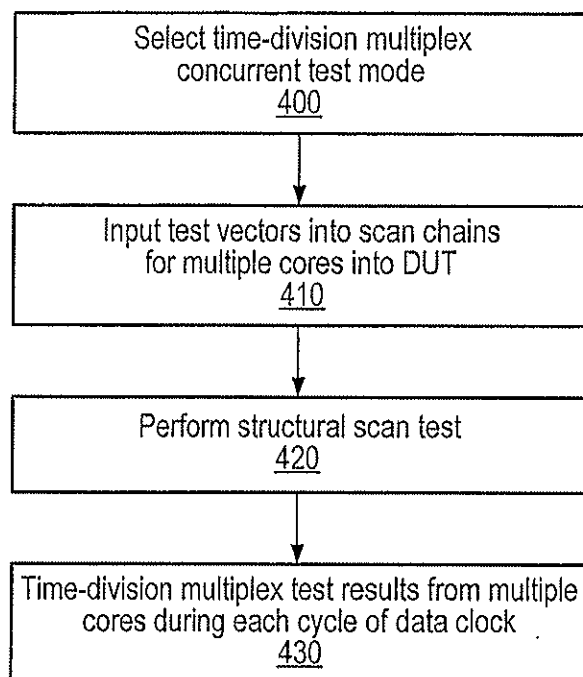


FIG. 4

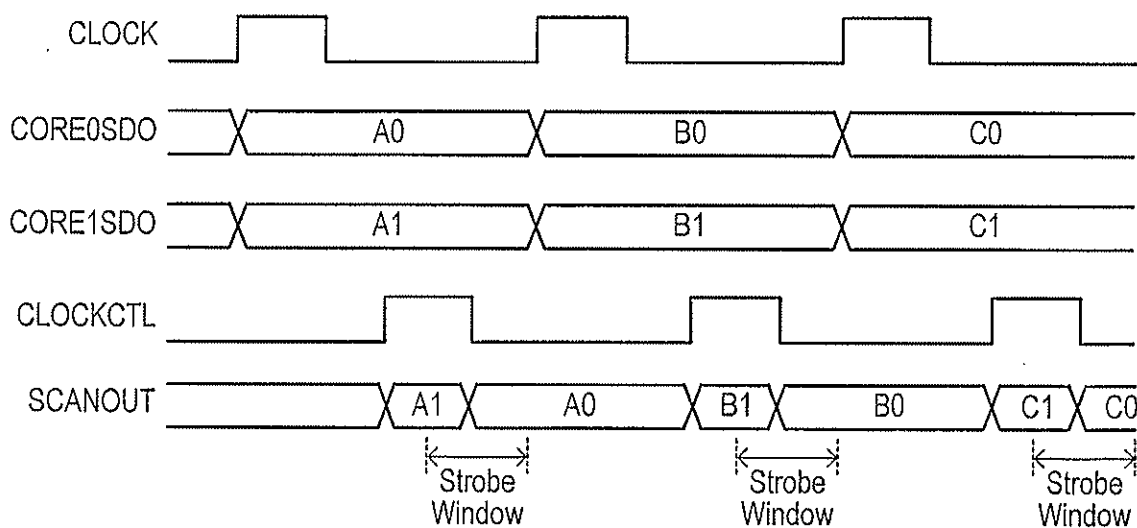


FIG. 5

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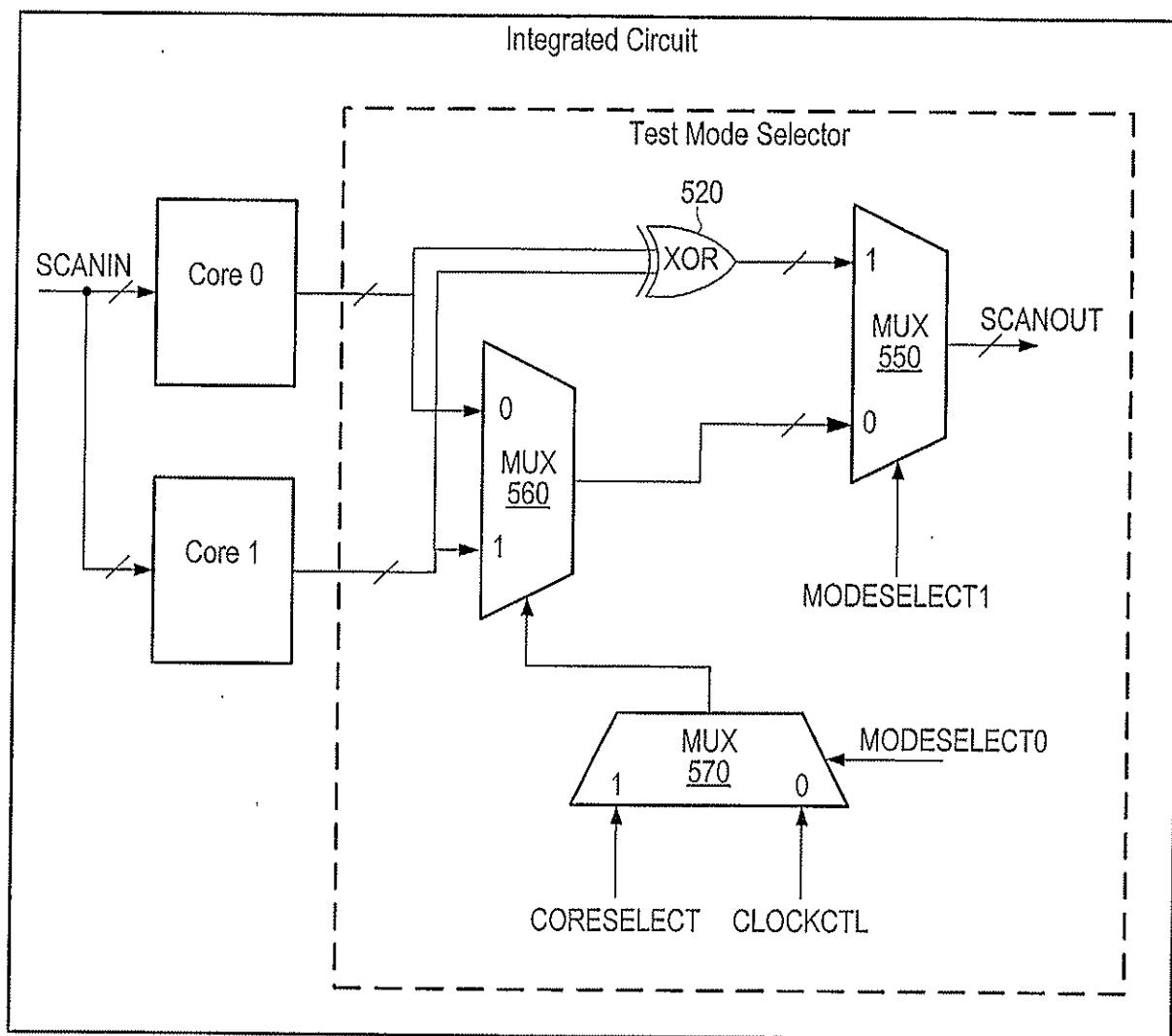


FIG. 6

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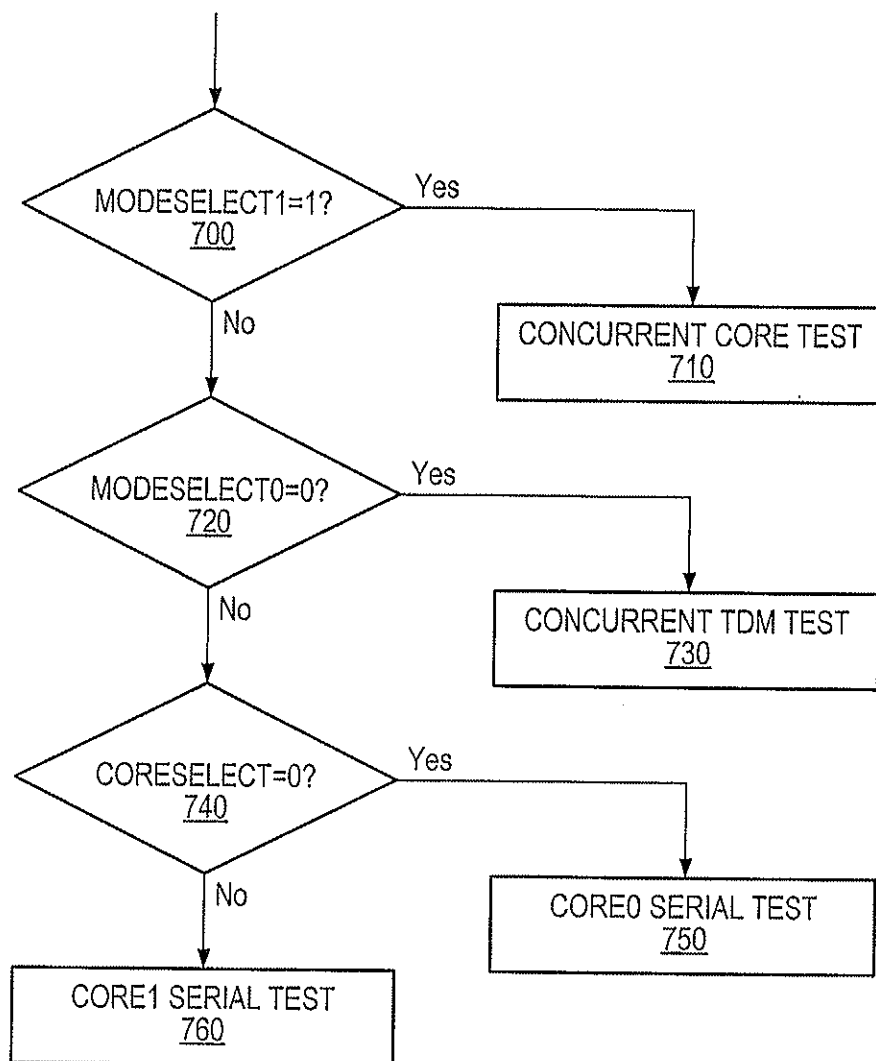


FIG. 7

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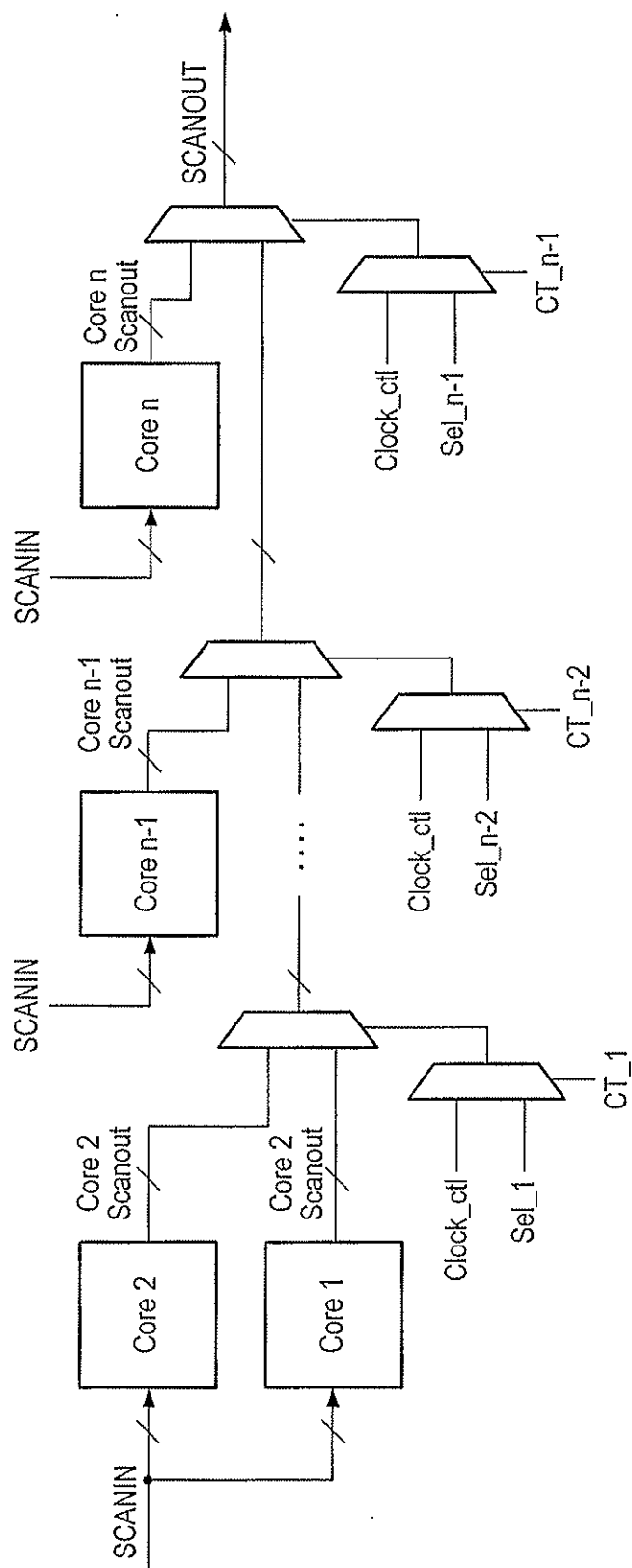


FIG. 8

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CT _{n-1}	CT _{n-2}	...	CT ₁	Sel _{n-1}	Sel _{n-2}	...	Sel ₁	Scan _{out}
0	0		0	0	0		0	Serial mode for Core 1
0	0		0	0	0		1	Serial mode for Core 2
		⋮					⋮	⋮
0	0		x	0	1		x	Serial mode for Core n-1
0	x		x	1	x		x	Serial mode for Core n
0	0		1	0	0		x	Concurrent TDM test mode for Core 1 and Core 2
		⋮					⋮	⋮
0	1		0	0	x		0	Concurrent TDM test mode for Core 1 and Core n-1
0	1		0	0	x		1	Concurrent TDM test mode for Core 2 and Core n-1
1	0		0	x	0		0	Concurrent TDM test mode for Core 1 and Core n
1	0		0	x	0		1	Concurrent TDM test mode for Core 2 and Core n
1	0		x	x	1		x	Concurrent TDM test mode for Core n-1 and Core n
								all other states are illegal

FIG. 9

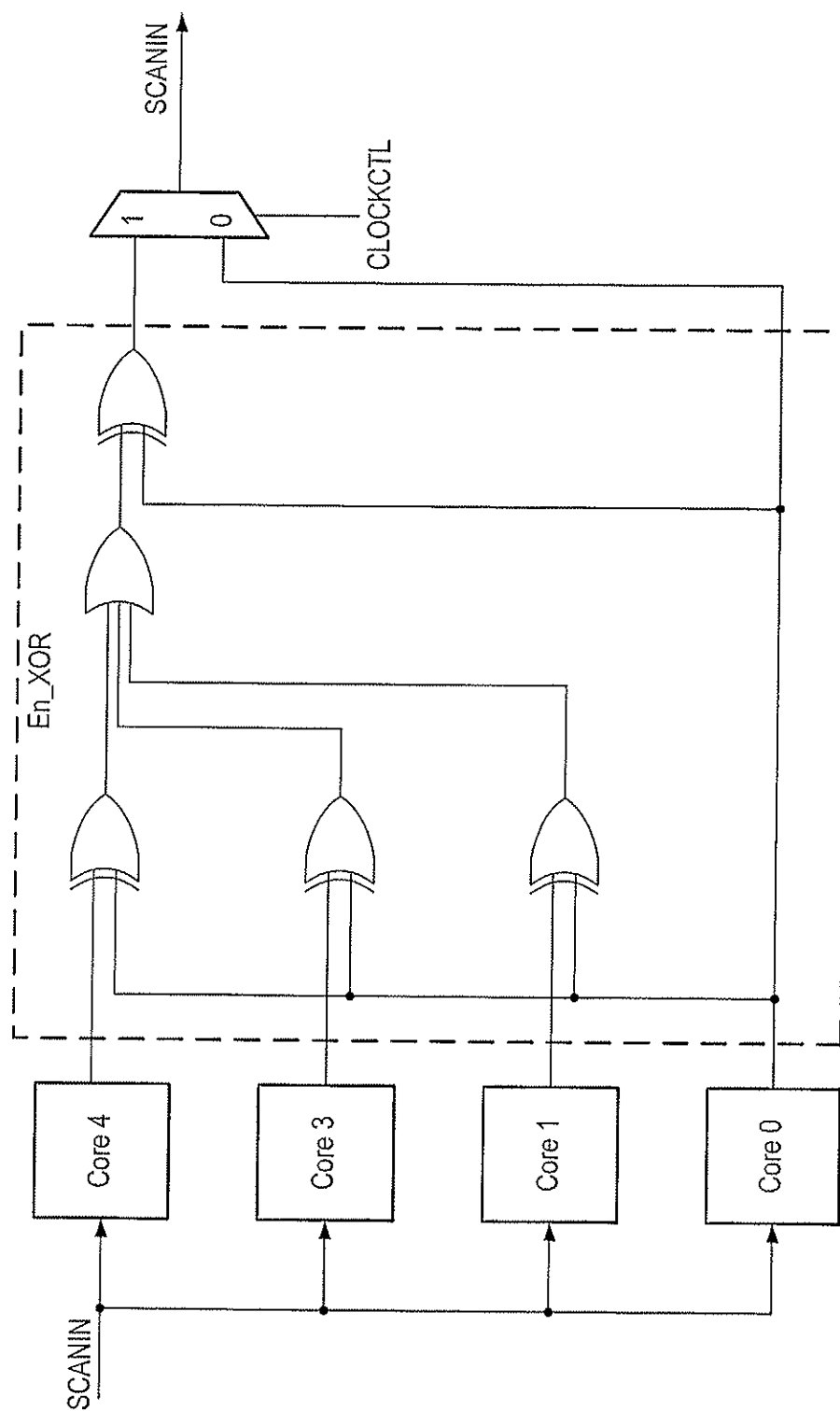


FIG. 10A

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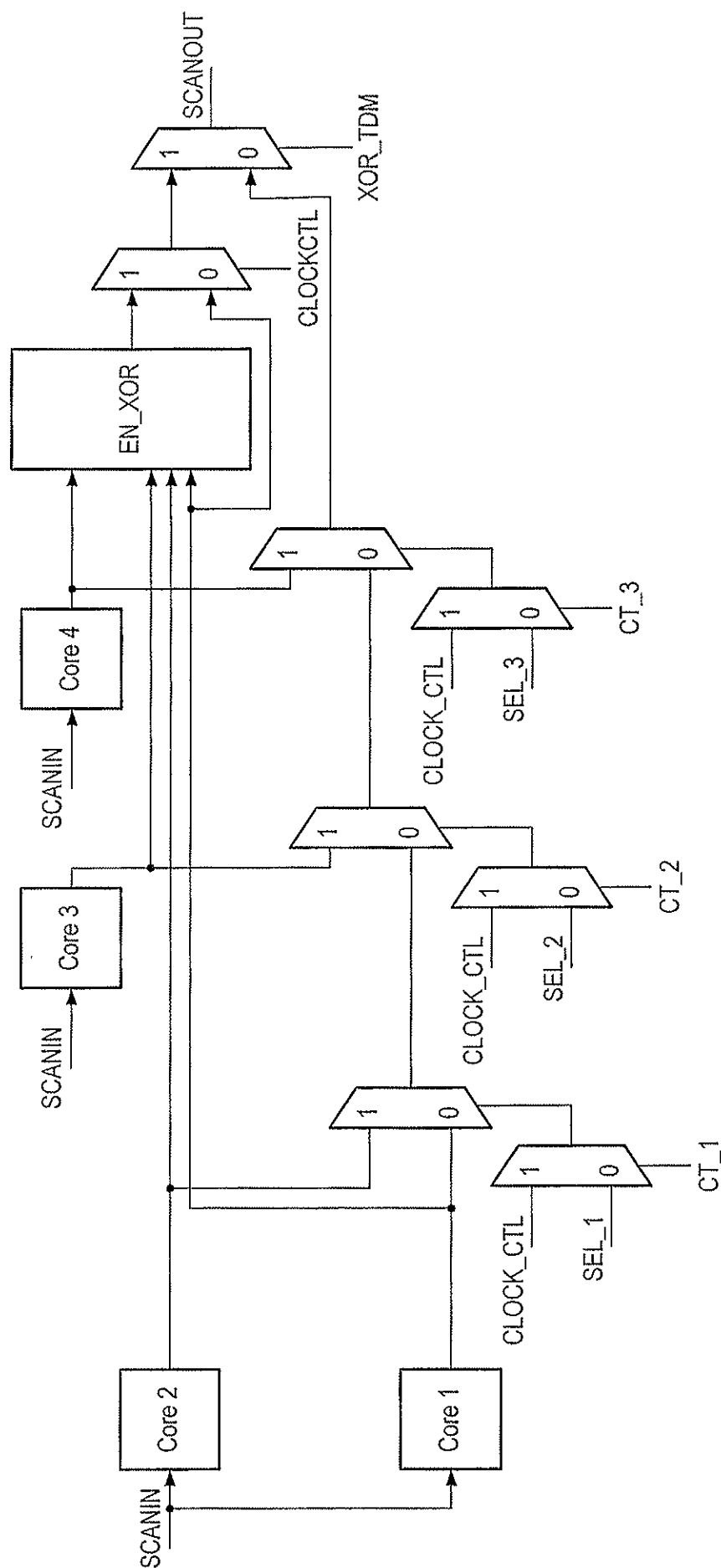


FIG. 10B

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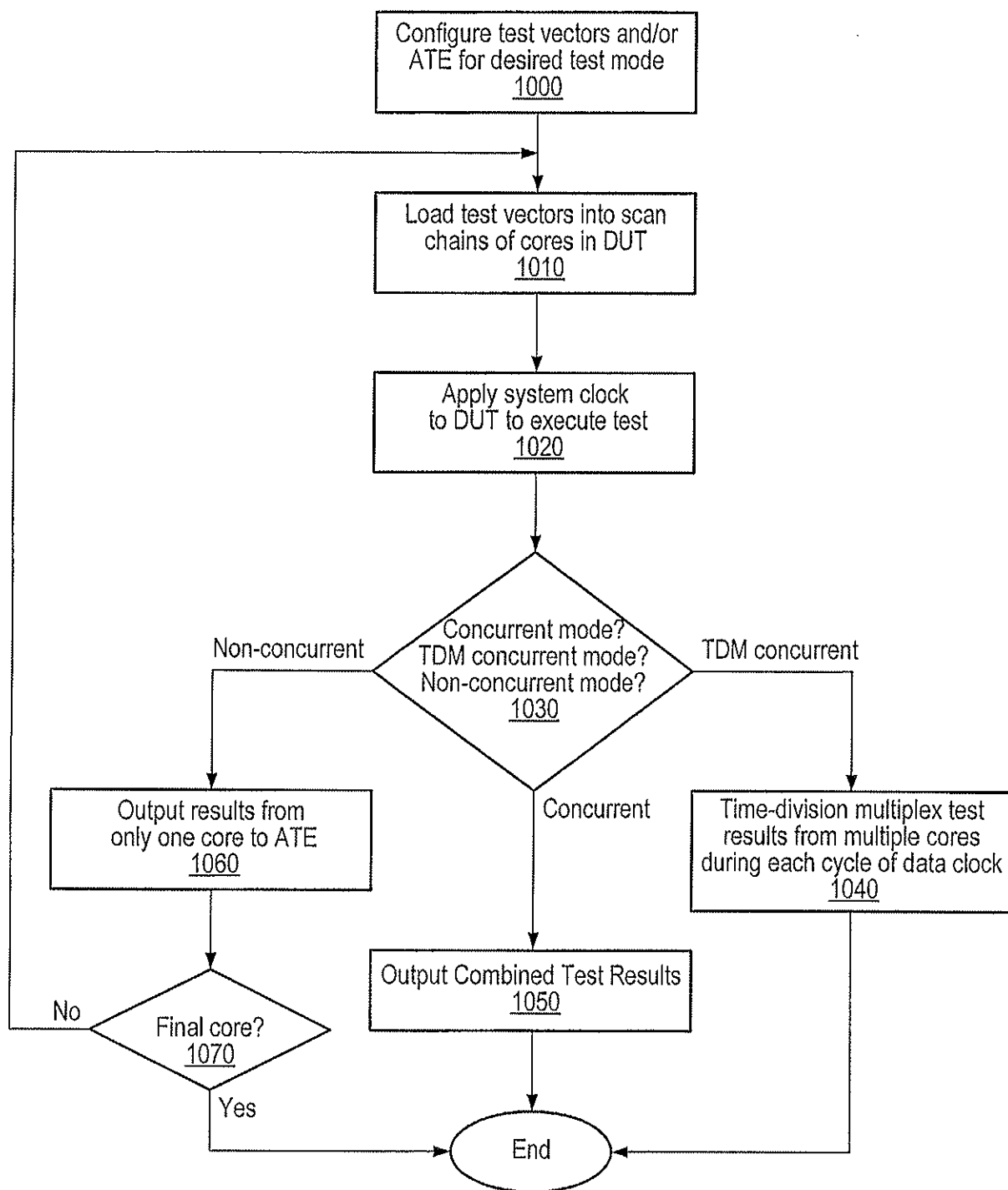


FIG. 11

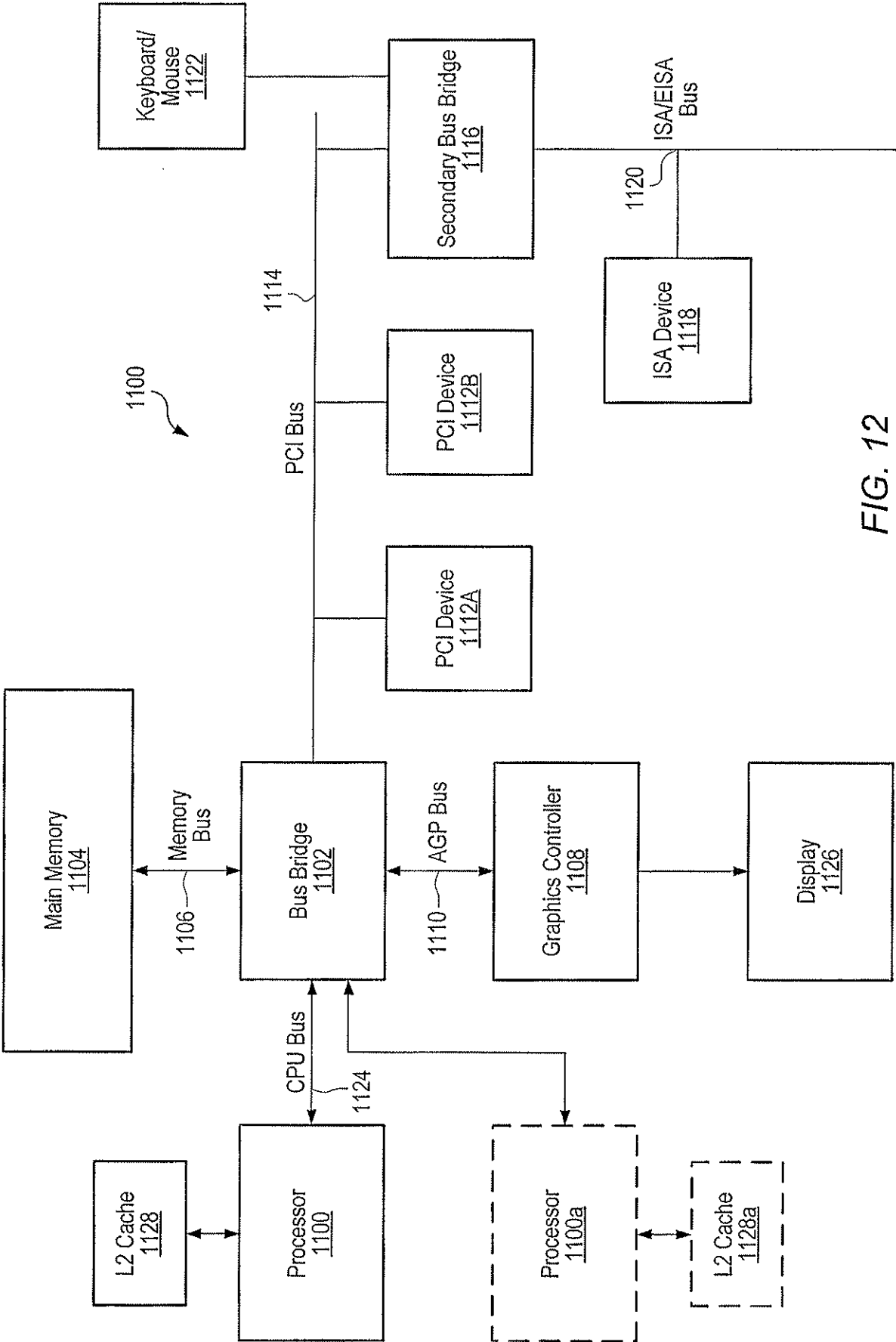


FIG. 12

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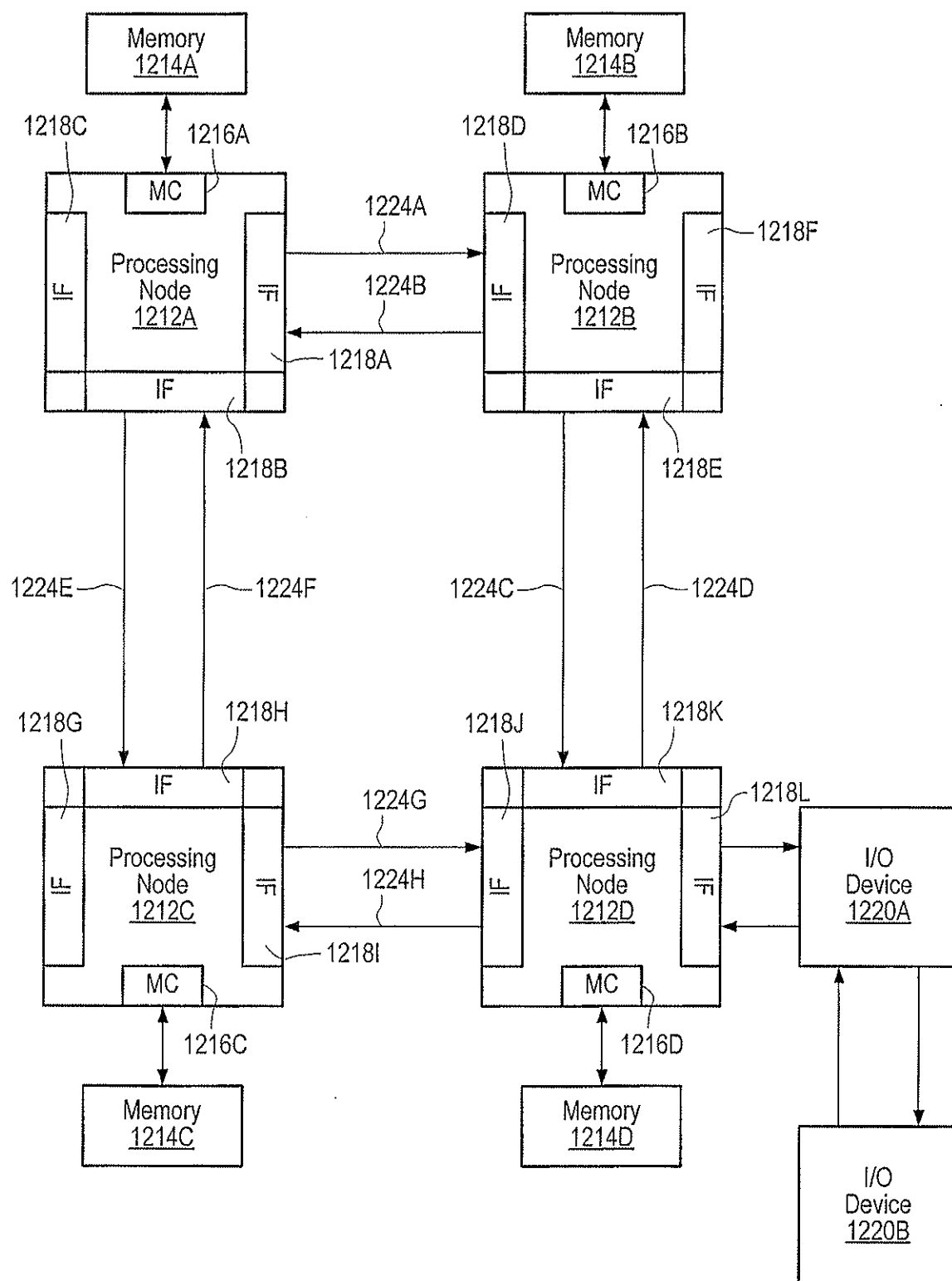


FIG. 13