

- 11 -

FPGA WITH DISTRIBUTED SWITCH MATRIX

Abstract

A field programmable gate array (FPGA) includes a distributed switch matrix for programmably connecting the various routing conductors. The distributed switch matrix comprises groups of additional conductors (e.g., 305, 306, 307), referred to as "Switching R-nodes". The Switching R-nodes programmably connect selected ones of the (e.g, horizontal) routing conductors (e.g., 301, 302, 303, 304) to other selected ones of the (e.g., vertical) routing conductors (e.g., 308, 309, 310, 311, 312). In this manner, the direct connection between the routing conductors may be avoided, allowing for a reduced number of programmable interconnect devices. In one preferred embodiment, a nibble-mode architecture is used, wherein four data conductors are provided for each group of routing conductors, with other multiples-of-four data conductors also being advantageous.

This Sheet Has Been Replaced

