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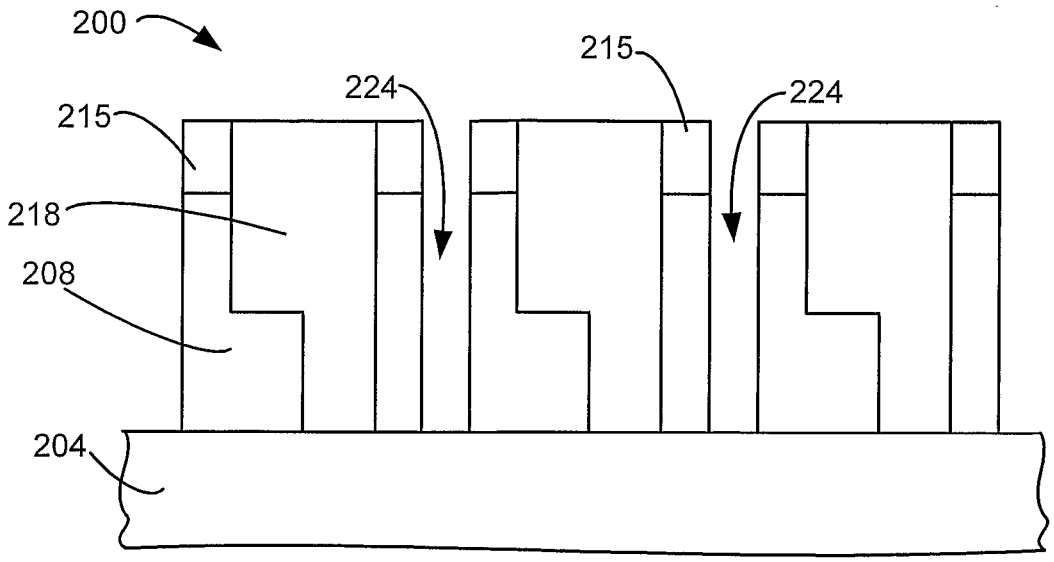
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(54) **Title:** DEVICE WITH SELF ALIGNED GAPS FOR CAPACITANCE REDUCTION



(57) **Abstract:** A method for reducing capacitances between semiconductor device wirings is provided. A sacrificial layer (212) is formed over a dielectric layer (208). A plurality of features (216) are etched into the sacrificial layer and dielectric layer. The features are filled with a filler material (218). The sacrificial layer is removed, so that parts of the filler material remain exposed above a surface of the dielectric layer, where spaces are between the exposed parts of the filler material, where the spaces (217) are in an area formerly occupied by the sacrificial layer. Widths of the spaces between the parts of the filler material are shrunk with a shrink sidewall deposition (215). Gaps (224) are etched into the dielectric layer through the shrink sidewall deposition. The filler material and shrink sidewall deposition are removed.

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