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HIGH VOLTAGE POWER INTEGRATED CIRCUIT WITH LEVEL SHIFT OPERATION AND WITHOUT METAL CROSSOVER

BACKGROUND OF THE INVENTION

High voltage power integrated circuits with means for producing level shifted signal outputs are well known. It is frequently necessary in such circuits to have a connector at high voltage cross over other connectors or semiconductor regions that are at a relatively lower voltage. This requires a thick dielectric between the regions of high potential, creating processing problems. The present invention provides a novel structure for eliminating the crossover connector (or conductor) for either a level shift up or level shift down structure.

Typical prior art devices in which the cross-over problem exists in the level shift up circuit is the IR2110 Power Integrated Circuit sold by the International Rectifier Corporation. In the IR2120 Power Integrated Circuit, a similar crossover problem exists in the level shift down circuit.

Figure 1 is a schematic diagram of the level shift up circuit in a die forming the prior art IR2110 device. There is schematically shown a ground referenced control circuit 1, a floating reference circuit 2 contained in a floating well of a common die, a pair of

high voltage level shift up MOSFETs 3, two high voltage metal "crossover" connectors 4 extending from the outputs of MOSFETs 3 and connected to the floating reference circuit 2 and a termination region 5 surrounding floating reference circuit 2 to isolate circuit 2 from the ground referenced control circuit 1. All of these circuits are integrated into a common silicon die or chip. Termination 5 of course, contains a blocking junction (not shown). Therefore, connectors 4 must cross over and be insulated from the blocking junction in region 5. For example, a dielectric as thick as 1.5 microns might be needed for products rated at about 500 to 600 volts. This thick dielectric causes serious manufacturing problems.

A similar problem exists with a level shift down circuit such as the circuit shown in the prior art circuit of Figure 2. In Figure 2, it will be noted that the level shift MOSFETs 3 are formed in the silicon within the floating reference circuit 2, rather than outside of the circuit 2 as in Figure 1. As in Figure 1, however, the connectors 4 must cross over the termination 5 and must be insulated from the high voltage across the termination region 5.

In more detail, and referring to Figure 1, the input to the chip is received on the ground referenced control circuit 1 side of the die. The input signal is processed and is sent forward through the level shift up MOSFETs 3 to the floating reference circuit 2 side. The high voltage crossover connectors 4 are needed to take the high voltage signal from the drains of the level shift FETs 3 to isolated floating well 2. Since connectors 4 cross over low voltage silicon, the dielectric material between the connectors 4 and the

silicon should be thick enough to withstand the full rated "Offset Voltage", between ground referenced and floating reference circuits 1 and 2, respectively. Consequently, in products such as the IR2110 and IR2120 parts, the dielectric is approximately 1.5 microns thick to ensure good yield for a rating of 500V. For a 1200V rating, as much as a 3 micron thick dielectric layer is needed. This causes many processing problems and is very difficult to control.

The same problem exists in the structure of Figure 2.

BRIEF DESCRIPTION OF THE INVENTION

In accordance with the invention, and to eliminate the high voltage crossover needed in the prior art, the level shift MOSFETs are built into the high voltage termination region. Thus, the need for a crossover conductor and a thick insulation layer is eliminated.

In accordance with the present invention, a level shift device electrically couples a floating voltage circuit with a relatively lower voltage circuit, each of which are formed on a common substrate of semiconductor material. A lightly doped layer of semiconductor material is disposed atop of the substrate and is of a first conductivity type. A base region of a second conductivity type is opposite to that of the first conductivity type extends into the upper surface of the layer to a given depth. A source region of the first conductivity type is formed in the base region and defines a surface channel region between the source region and the layer of semiconductor material. A source electrode is connected to the source region and is

electrically coupled to the lower voltage circuit. A gate insulation layer is disposed over the channel region, and a conductive layer is disposed over the gate insulation layer. A drain contact diffusion region of the first conductivity type is formed in the upper surface and is laterally spaced away from the base region. A drain electrode is connected to the drain contact diffusion region. A further diffusion region of the first conductivity type is formed in the upper surface of the layer of semiconductor material and is laterally spaced away from the drain region and further away from the base region. The portion of the layer of semiconductor material that is located between the base region and the further diffusion region defines a conduction region. An insulating layer is formed atop the upper surface of the layer of semiconductor material, between the drain region and the further diffusion region. A contact electrode is formed atop the further diffusion region and is electrically coupled to the floating voltage circuit. A conducting resistor layer is located over the insulating layer between the drain electrode and the contact electrode and defines a resistor that is arranged electrically parallel with the conduction region of the layer of semiconductor material. The resistance of the conduction region is greater than the resistance of the conductive resistor layer.

A diffusion region of the second conductivity type may be formed in the upper surface of the layer of semiconductor material to a predetermined depth and located beneath the insulating layer such that the conduction region is reduced. Another body region of a second conductivity type may be formed in the upper surface of the layer of semiconductor material and

disposed between the body region and the drain contact diffusion region. A further metal contact may be disposed atop at least a portion of this additional body region and may be electrically connected to the source electrode. A resurf region of the second conductivity type may be formed in the upper surface of the layer of semiconductor material and disposed between the second body region and the drain region in contact with the additional body region.

The source contact region may further contact a portion of the body region. A heavily doped base region of the second conductivity type may be formed in a layer of semiconductor material and extend into the substrate thereby electrically isolating the device.

According to another aspect of the invention, an integrated circuit includes a floating voltage circuit, a relatively lower voltage circuit and a level shift device formed in a common substrate with the floating voltage circuit and the lower voltage circuit.

According to a further aspect of the invention a high voltage MOSFET device electrically couples a floating voltage circuit and a relatively lower voltage circuit which are each formed in a common substrate with the MOSFET device. A layer of semiconductor material of the first conductivity type is disposed above the substrate and is lightly doped and has an upper surface. A source diffusion region of the second conductivity type opposite that of the first conductivity type is formed in the upper surface of the layer of semiconductor material. A source electrode is connected to the source region. A gate insulation layer is disposed over a portion of the upper surface of the layer of semiconductor material adjacent to the source diffusion region, and a conductive

gate layer is disposed over the gate insulation layer. A drain region of the second conductivity type is formed in the upper surface of the layer of semiconductor material and is laterally spaced away from the source diffusion region. A drain electrode is disposed atop the drain diffusion. A sinker region of the second conductivity type extends from the upper surface of the layer of semiconductor material and extends into the substrate and is laterally spaced away from the drain region and further spaced away from the source diffusion. A ground electrode is connected to the sinker region. An insulating layer is disposed atop the upper surface of the layer of semiconductor material between the drain electrode and the ground electrode. A conductive resistor layer is disposed atop the insulating layer and is connected between the ground electrode and the drain electrode. The source electrode is electrically coupled to the floating voltage circuit and the drain electrode is electrically coupled to the lower voltage circuit.

An isolation diffusion region of the second conductivity type may be formed in the upper surface and contact the sinker region and be located beneath the insulating layer and laterally spaced away from the drain region to reduce parasitic resistances. A lightly doped resurf region may be formed in the upper surface in contact with the drain region and arranged between the drain region and the source diffusion region. A further diffusion region of the first conductivity type may be formed in the upper surface of the layer of semiconductor material and contact the source diffusion region and the source electrode. At least one gap may be formed in the sinker diffusion region.

According to a still further aspect of the present invention an integrated circuit includes a floating voltage circuit formed in a substrate, a resurf diffusion region substantially surrounding the floating voltage circuit, a relatively lower voltage circuit formed in the substrate, and at least one level shift MOSFET device formed in the substrate and electrically coupled between the high voltage circuit and the low voltage circuit. The MOSFET device is formed in a gap disposed in the resurf region.

According to yet another aspect of the invention, an integrated circuit includes a floating voltage circuit formed in a substrate, a resurf diffusion region that encloses the high voltage circuit, a relatively lower voltage circuit that is formed in the substrate, and at least one level shift MOSFET device formed in the substrate and electrically coupled between the high voltage circuit and the low voltage circuit. The resurf region at least partially encloses the level shift MOSFET device and is disposed between the level shift MOSFET device and the floating voltage device.

A further conductive resistor layer may be connected between the drain electrode and the ground electrode and parallel with a conductive resistor layer.

Other features and advantages of the invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a prior art level shift up circuit.

Figure 2 is a schematic diagram of a prior art level shift-down circuit.

Figure 3 is a schematic diagram of the level shift up circuit of Figure 1 when modified to incorporate the present invention.

Figure 4 is a cross-section of Figure 3 taken across section line 4-4 in a die used for the structure of Figure 3.

Figure 5 is a cross-section of Figure 3 taken across section line 5-5 in Figure 3.

Figure 6 is a schematic diagram of the structure of Figures 3 and 4.

Figure 7 is a schematic diagram of a level shift down circuit, when modified to incorporate the present invention.

Figure 8 is a cross-sectional view of Figure 7, taken across the section line 8-8 in Figure 7.

Figure 9 is a circuit diagram of the level shift down MOSFET in Figures 7 and 8.

Figure 10 shows a modification of Figure 7, with a reshaped termination topology.

Figure 11 is a cross-section of Figure 10 taken across section line 11-11 in Figure 10.

Figure 12 is a diagram of the circuit of the structure of Figures 10 and 11.

Figure 13 shows an embodiment of the invention using a single high voltage PMOS device.

Figure 14 is a circuit diagram that illustrates the parasitic resistance between the drains of two level shift MOSFETs formed in a common epitaxial region.

Figure 15 shows another embodiment of the invention in which the level shift circuits are formed in respective separate epitaxial regions.

DETAILED DESCRIPTION OF THIS INVENTION

The present invention eliminates the need for the crossover 4 of Figure 1 for the level shift up circuit of Figure 1 as shown in Figures 3, 4, and 6. Essentially the new design combines the level shift MOSFETs 3 with the high voltage termination 5. In this way, the need for any high voltage crossover connector is eliminated.

Figure 4, which is a cross-section of Figure 3 at section line 4-4 in Figure 3, shows a small portion of the integrated circuit chip, and shows the silicon P type substrate 11 (which may have a resistivity of 10 to 200 ohm cm) and which has an N^- epitaxially deposited layer 10 concentric thereon. Ring-shaped P type body regions 12 and 16 are diffused into layer 10 and a source ring 13 is diffused into body 12. A polysilicon gate 14 is deposited atop a conventional gate oxide and covered by an oxide "cap" 15 (conventionally a low temperature oxide) which extends across the channel in body 12 formed by source 13 to define the N channel MOSFET 3 (Figures 1 and 6). Ring-shaped diffusion 16 increases device ruggedness.

The N^- epitaxial body 10 of Figure 4 also receives a P^- resurf region 30. Low temperature oxide 31, which may contain known spaced voltage dividing polysilicon plates (not shown), may be contained within oxide 31. Such plates are shown in U.S. Patent No. 5,270,568.

A P^+ sinker 40 is used to segregate separate devices or integrated circuit wells within the common silicon chip 11. An aluminum source metal 41 is connected to define the MOSFET 3 source, while its drain is defined by the metallization 42 which defines an

output drain terminal 43. P body 16 also receives a metal contact 41a which is suitably connected to source metallizing 41. An N^+ diffusion 44 is provided to enable good contact between metal 42 and N^- epi 10.

In accordance with an important feature of the invention, a polysilicon resistor 50 (sometimes referred to as R_{POLY}) is deposited atop a field oxide layer 51 (which is covered by a suitable low temperature oxide layer) and is connected at one end to metal 42 and at its other end to high voltage metal 53. Metal 53 is connected to silicon 10 via the N^+ diffusion 54. It should be noted that the function of poly resistor 50 could be implemented on other ways, and could, for example, be formed of a diffused P region in the N^- epi 10.

A P^+ region 60 is formed under oxide 51 to increase the length of the majority carrier path between diffusions 44 and 54. That is, the resistance of the path beneath the P^+ region 60 in the N^- epi 10 has a resistance R_{epi}. The diffusion 60 increases the value R_{epi} by pinching the available conduction area in N^-_{epi} 10 between the P^- substrate 11 and the P^+ region 60. The added resistor formed by R_{POLY} 50 makes the circuit operate more predictably since it reduces the effect of the variability of R_{epi} which changes as a function of the value of the voltage HV due to depletion effects in the epitaxial layer.

The circuit relationship between R_{POLY} 50 and R_{epi} is shown in Figure 6. At higher voltage, the depletion region extends further into the epitaxial layer, causing the effective R_{epi} to increase dramatically. The higher value of the level shift resistor makes the circuit more

sensitive to dv/dt related malfunctions. Typically, R_{POLY} 50 is about 1,000 ohms while R_{epi} varies from 3,000 ohms at zero bias to a higher effective resistance at high voltage.

Figure 5 shows the termination 5 of Figure 3, which consists of a pair of P^+ sinkers 70 and 71 in epi 10. Grounded metal layers 72 and 73 respectively are atop sinkers 70 and 71, and N^+ diffusion 77 receives a metal strip 76. Note that high voltage metal does not extend across the termination. Resurf regions 74 and 75 may also be provided.

The ring shaped P type body regions of the level shift MOSFETs of Figs. 3-6 minimize the cross-talk that is present when more than level shift circuit is connected to the same floating circuit. This cross-talk is caused by the presence of the drain terminals in the same epitaxial island, which results in the drains being connected to each other through the parasitic resistance of the epitaxial layer. This type of cross-talk does not occur in the prior art level shift circuit, such as is shown in Fig. 2, where the drains of the respective level shift MOSFETs are located in separate epitaxial layer islands and are isolated from each other.

The parasitic resistance between the level shift MOSFETs of Figs. 3-6 is shown in Fig. 14 in which a parasitic resistance 94 is formed between the respective drains of MOSFETs 90 and 92. The parasitic resistance causes a current to flow through resistor 96 whenever MOSFET 90 is activated and can cause false triggering in the floating circuit connected to output2 even when MOSFET 92 is not activated. Similarly, a current can flow through resistor 98 when MOSFET 92 is activated.

The amount of cross-talk depends on the relative values of resistors 96 and 94 when MOSFET 90 is activated, and depends on the relative values of resistors 98 and 94 when MOSFET 92 is activated. Thus the resistance of resistor 94 should be as high as possible to minimize cross-talk. In the level shift circuits shown in Figs. 3-6, the problem of cross-talk is minimized by forming P type body regions 12 and 16 that maximize the resistance of resistor 94.

Alternatively, the cross-talk problem can be minimized by physically separating the two level shift MOSFETs, as shown in Fig. 15.

To summarize, the salient features of the improvements of Figures 3 to 6 are:

1. No high voltage metal crossover by virtue of the layout.
2. An additional level shift resistor 50 (diffused or poly) in parallel with the resistor R_{epi} provides more stable operation of the circuit over a wider range of applied high voltage.
3. Since the R_{epi} is essentially a parasitic element, its effect is minimized by maximizing the distance between N^+ diffusions 44 and 54.
4. The added P type diffusion 60 between diffusions 44 and 54 minimizes the effect of R_{epi}.
5. The cross-talk among the level-shift MOSFETs within the same floating reference circuit is minimized by providing a ring shaped P type body region as shown in Figure 3 or by separating the level shift circuits from one another.

Referring next to Figure 7, there is shown a schematic diagram like that of Figure 2, but in which the P resurf diffusion portion of region 5 is interrupted at

gaps 201, 202 and 203 which may be small, for example, 5 microns each. The silicon chip is then diffused, as shown in Figure 8, to define the source, gate and drain regions for lateral high voltage PMOS FETs 3 of Figure 7. Thus, in Figure 8, numerals similar to those of Figure 5 designate like components.

It will be noted in Figure 8 that a P^+ region 209 extends from sinker 40 and underlies LTO layer 210. A P^+ drain diffusion 211 receives drain contact 212 and P^- resurf diffusion 213 extends from region 211. A source contact 214 contacts P^+ diffusion 220 and N^+ contact diffusion 221. A polysilicon gate 222 overlies the surface of the N^- epi material exposed between P^- resurf region 213 and P^+ region 220. LTO regions 223 and 224 cross over and seal the upper device surface as shown. A polysilicon resistor 225 connects ground contact 226 to drain contact 212.

The resulting device is a high voltage PMOSFET down shift circuit having the circuit diagram shown in Figure 9. Significantly, the high voltage crossover 4 of Figure 2 is eliminated.

Also, by spacing the P^+ drain 211 from the isolation diffusion 209, the parasitic resistance (R_{RSF} in Figure 12) is eliminated. Note that this small space is easily depleted at high voltage.

Figure 10 shows another embodiment of a termination region which, as in Figure 3, is "looped" to increase its length in the area of the level shift MOSFETs. This loop topology also significantly reduces "cross-talk" between the drains of the two MOSFET drains 240a and 241c in Figure 10 by maximizing the parasitic resistance R_{CP} shown in Figure 14.

Thus, two "loops" 240 and 241 are provided in Figure 10. The PMOSFETs in these regions are shown in Figure 11 for a region 240 that includes source region 220. Like numerals in Figure 11 describe like components of Figure 8. Note that the P^- region 250 is extended and contacts drain region 211 in Figure 11. The loops 240 and 241 make the effective value of the parasitic resistance of region 250 as high as possible, thereby to make the resistance of poly resistor 225 the dominant resistor, as shown in Figure 12.

Figure 13 shows the invention for a single down level shifter PMOSFET for the device of Figures 7 and 8. Thus, only two gaps 300 and 301 define the high voltage PMOSFET 302. Gaps 300 and 301 are preferably typically 5 microns wide and are small enough to be self isolating. The high voltage diode similar to that is shown in Figure 5, while the PMOSFET at section lines 8-8 is shown in Figure 8. Other numerals in Figure 13 identify like components of Figures 7 and 8.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

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WHAT IS CLAIMED IS:

1. A level shift device for electrically coupling a floating voltage circuit with a relatively lower voltage circuit each formed on a common substrate of semiconductor material with said level shift circuit, said level shift circuit comprising:

a layer of semiconductor material disposed atop said substrate, said semiconductor material being of a first conductivity type and being lightly doped and having an upper surface;

a base region of a second conductivity type opposite to that of said first conductivity type, said base region extending into the upper surface of said layer of semiconductor material to a given depth and having a substantially semicircular configuration;

a source region of said first conductivity type formed in said base region and defining a surface channel region between said source region and said layer of semiconductor material;

a source electrode connected to said source region and electrically coupled to said lower voltage circuit;

a gate insulation layer disposed over said channel region;

a conductive gate layer disposed over said gate insulation layer;

a drain electrode connected to a portion of said layer of semiconductor material thereby defining a drain region, said drain electrode being laterally spaced away from said base region;

a contact electrode connected to another portion of said layer of semiconductor material and

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electrically coupled to said floating voltage circuit, the portion of said layer of semiconductor material located between said drain electrode and said contact electrode defining a conduction region; and

a resistor disposed between said drain electrode and said contact electrode, said resistor being arranged electrically parallel with said conduction region of said layer of semiconductor material.

2. The device of claim 1 wherein said resistor comprises a diffusion region of said second conductivity type formed in said upper surface of said layer of semiconductor material to a predetermined depth.

3. The device of claim 1 further comprising another substantially semicircular body region of said second conductivity type formed in said upper surface of said layer of semiconductor material concentric with said body region and disposed between said body region and said drain electrode.

4. The device of claim 3 further comprising a further metal contact disposed atop at least a portion of said another body region.

5. The device of claim 4 wherein said further metal contact is electrically connected to said source electrode.

6. The device of claim 1 further comprising a resurf region of said second conductivity type formed in said upper surface of said layer of semiconductor material and disposed between said another body region

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and said drain diffusion region and in contact with said another body region.

7. The device of claim 1 wherein said resistor is a conducting layer disposed atop an insulating layer.

8. The device of claim 1 further comprising a heavily doped spacer region of said second conductivity type formed in said layer of semiconductor material and extending into the substrate for electrically isolating said device.

9. An integrated circuit comprising a floating voltage circuit; a relatively lower voltage circuit; and a level shift device comprising the device of claims 1, 2, 3, 4, 5, 6, 7 or 8.

10. A device for electrically coupling a floating voltage circuit with a relatively lower voltage circuit each formed in a common substrate with said MOSFET device, said MOSFET device comprising:

a layer of semiconductor material of first conductivity type disposed atop said substrate and being lightly doped and having an upper surface;

a source diffusion region of said second conductivity type opposite to that of said first conductivity type and formed in said upper surface of said layer of semiconductor material;

a source electrode connected to said source region and electrically coupled to said floating voltage circuit;

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a gate insulation layer disposed over a portion of said upper surface of said layer of semiconductor material adjacent to said source diffusion region;

a conductive gate layer disposed over said gate insulation layer;

a drain region of said second conductivity type formed in said upper surface of said layer of semiconductor material and being laterally spaced away from said source diffusion region;

a drain electrode disposed atop said drain diffusion and electrically coupled to said lower voltage circuit; and

a resistor connected between said ground electrode and said drain electrode.

11. The device of claim 10 further comprising a sinker region of said second conductivity type extending from said upper surface of said layer of semiconductor material and extending into said substrate and being laterally spaced away from said drain region and being further spaced away from said source diffusion; and

a ground electrode connected to said sinker region.

12. The device of claim 11 further comprising an isolation diffusion region of said second conductivity type formed in said upper surface of said layer of semiconductor material and contacting said sinker region and being laterally spaced away from said drain region to reduce parasitic resistances.

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13. The device of claim 10 further comprising a lightly doped resurf region formed in said upper surface of said layer of semiconductor material in contact with said drain region and being arranged between said drain region and said source diffusion region.

14. The device of claim 10 further comprising a further diffusion region of said first conductivity type formed in said upper surface of said layer of semiconductor material and contacting said source diffusion region and said source electrode.

15. An integrated circuit comprising a floating voltage circuit formed in a substrate; a resurf diffusion region substantially surrounding said floating voltage circuit; a relatively lower voltage circuit formed in said substrate; and at least one level shift MOSFET device comprising the device of claims 10, 11, 12, 13 or 14.

16. A device for electrically coupling a floating voltage circuit with a relatively lower voltage circuit each formed in a common substrate with said MOSFET device, said MOSFET device comprising:

a layer of semiconductor material of first conductivity type disposed atop said substrate and being lightly doped and having an upper surface;

a source diffusion region of said second conductivity type opposite to that of said first conductivity type, said source diffusion region being formed in said upper surface of said layer of semiconductor material and having a substantially semicircular configuration;

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a source electrode connected to said source region and electrically coupled to said floating voltage circuit;

a gate insulation layer disposed over a portion of said upper surface of said layer of semiconductor material adjacent to said source diffusion region;

a conductive gate layer disposed over said gate insulation layer;

a drain region of said second conductivity type formed in said upper surface of said layer of semiconductor material and being laterally spaced away from said source diffusion region;

a drain electrode disposed atop said drain diffusion and electrically coupled to said lower voltage circuit; and

a resistor connected between said ground electrode and said drain electrode.

17. The device of claim 16 further comprising a sinker region of said second conductivity type extending from said upper surface of said layer of semiconductor material and extending into said substrate and being laterally spaced away from said drain region and being further spaced away from said source diffusion; and

a ground electrode connected to said sinker region.

18. The device of claim 17 further comprising an isolation diffusion region of said second conductivity type formed in said upper surface of said layer of semiconductor material and contacting said sinker region and said drain region.

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19. The device of claim 16 further comprising a lightly doped resurf region formed in said upper surface of said layer of semiconductor material in contact with said drain region and being arranged between said drain region and said source diffusion region.

20. The device of claim 16 further comprising a further diffusion region of said first conductivity type formed in said upper surface of said layer of semiconductor material and contacting said source diffusion region and said source electrode.

21. An integrated circuit comprising a floating voltage circuit formed in a substrate; a resurf diffusion region enclosing said high voltage circuit; a relatively lower voltage circuit formed in said substrate; and at least one level shift MOSFET device formed in said substrate and electrically coupled between said high voltage circuit and said low voltage circuit, said resurf region at least partially enclosing said level shift MOSFET device and disposed between said level shift MOSFET device and said floating voltage device; said MOSFET device comprising the device of claims 16, 17, 18, 19 or 20.

22. The integrated circuit of claim 21 further comprising a further diffusion region of said second conductivity type formed in said upper surface of said layer of semiconductor material and disposed between and contacting said resurf region and said drain region.

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23. The integrated circuit of claim 22 wherein said further diffusion region comprises a further conductive resistor connected between said drain electrode and said ground electrode in parallel with said conductive resistor layer.

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HIGH VOLTAGE POWER INTEGRATED CIRCUIT WITH LEVEL SHIFT OPERATION AND WITHOUT METAL CROSSOVER

ABSTRACT OF THE DISCLOSURE

Level shift devices are formed in the high voltage termination region of an integrated circuit. The level shift devices provide a connection between the higher voltage, floating circuit and a ground referenced lower voltage circuit. The structure of the level shift devices eliminates the need for a high voltage connector to cross over the low voltage connector.

Fig. 4

FIG. 1 (PRIOR ART)

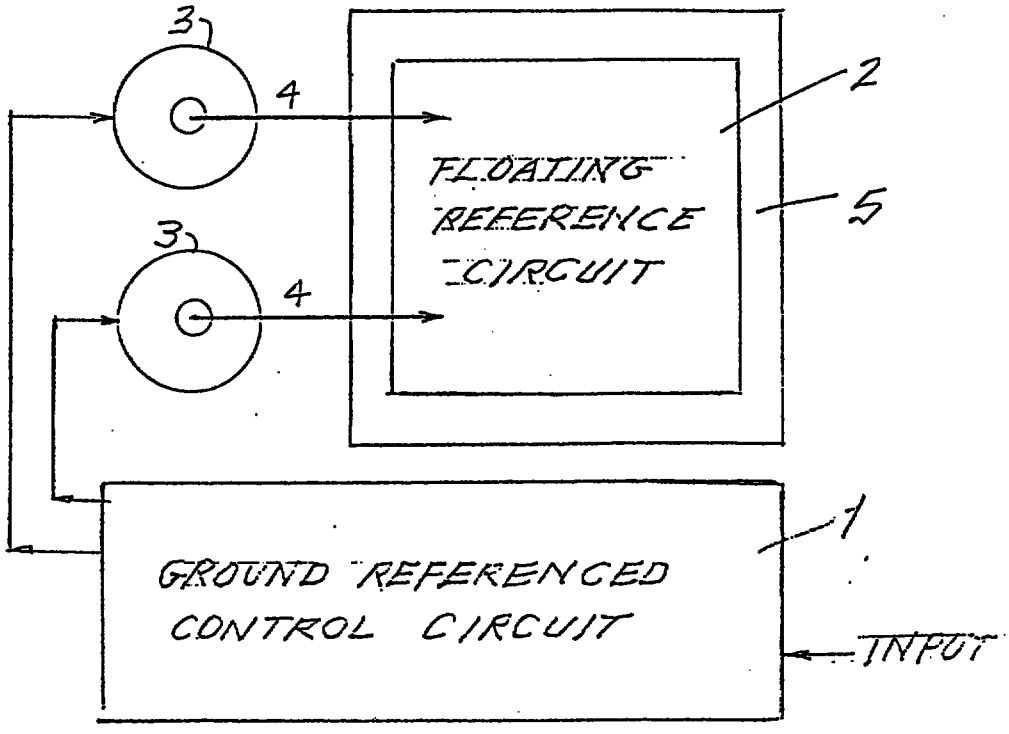
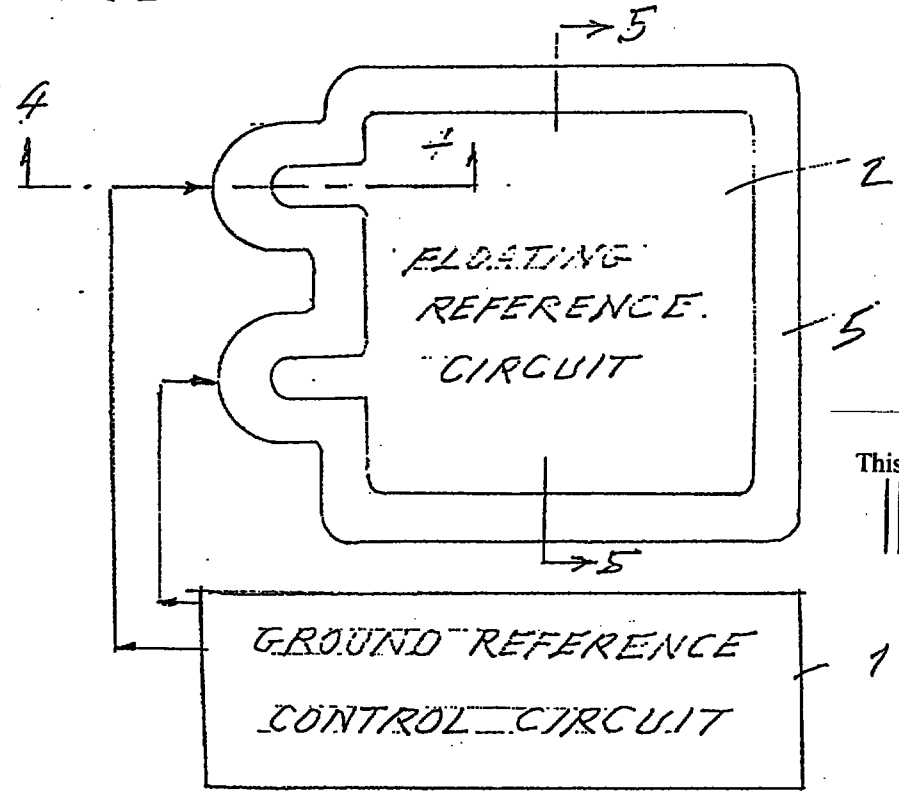
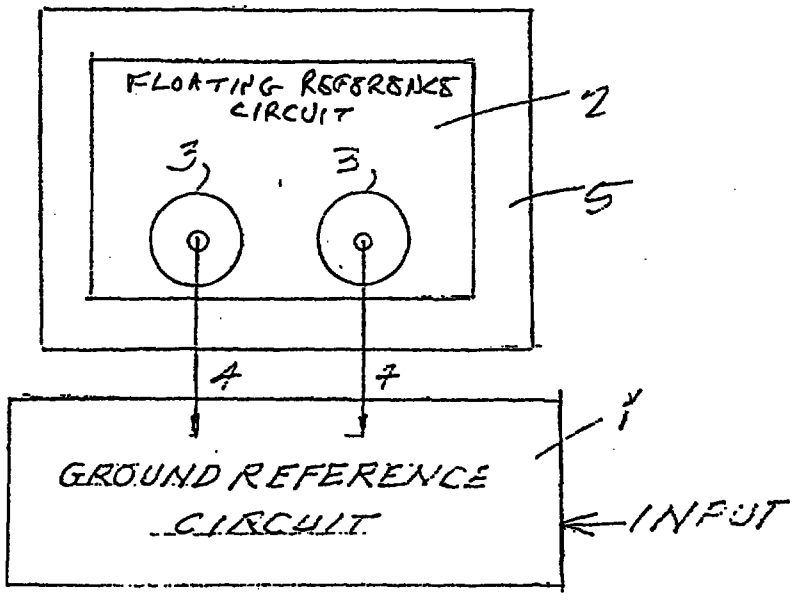


FIG. 2



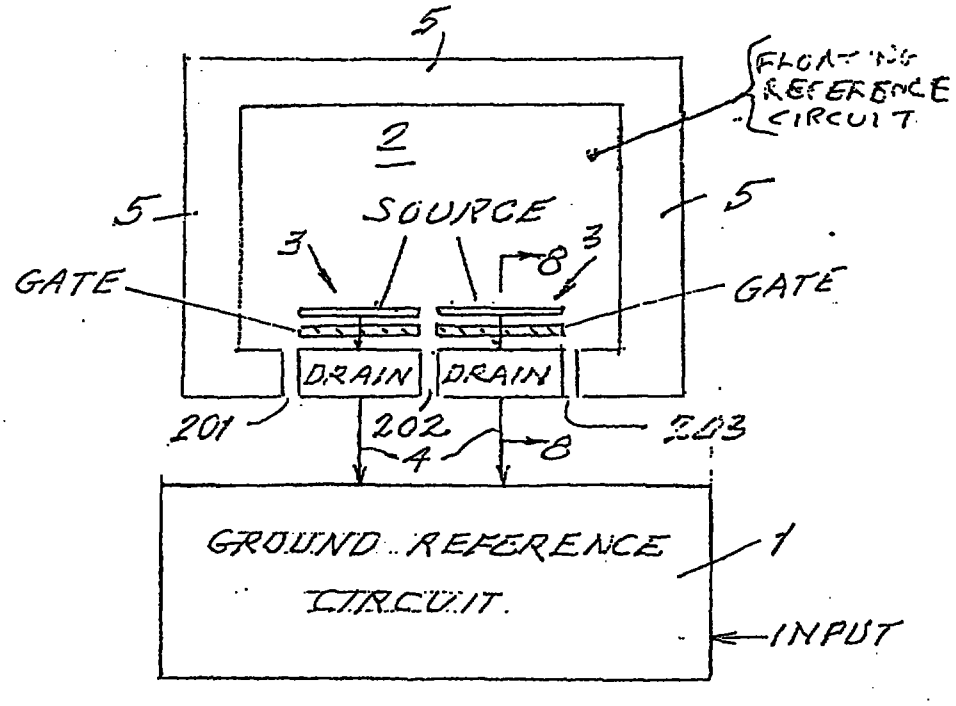
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FIG. 2. PRIOR ART



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FIG. 7



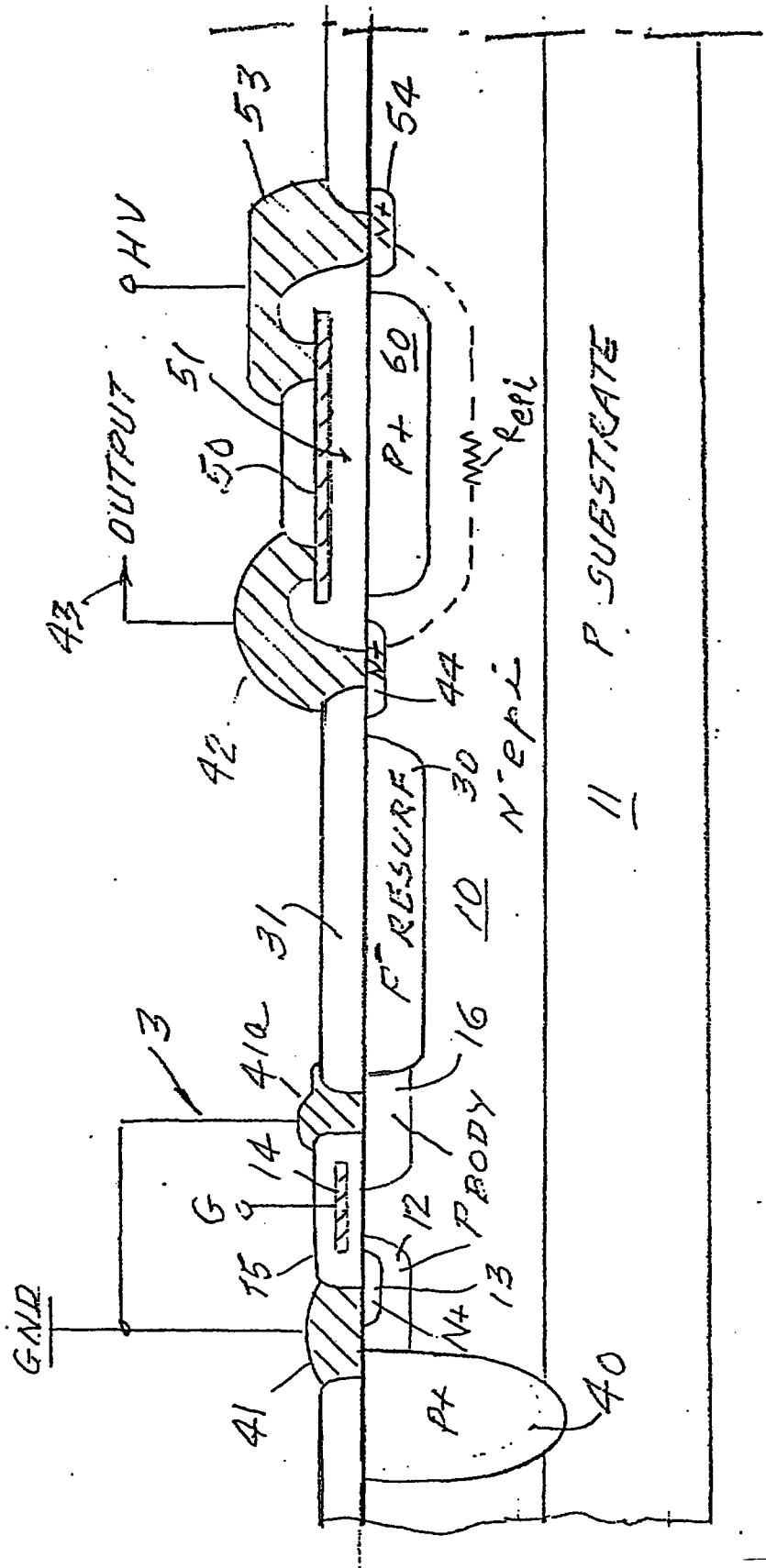


FIG 4

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FIG. 5

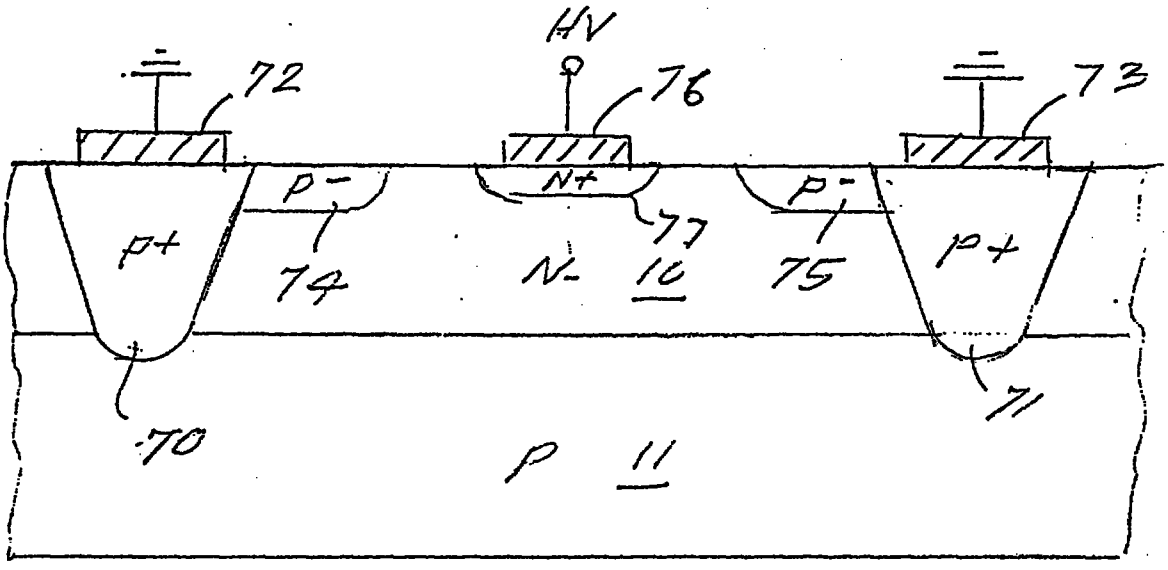
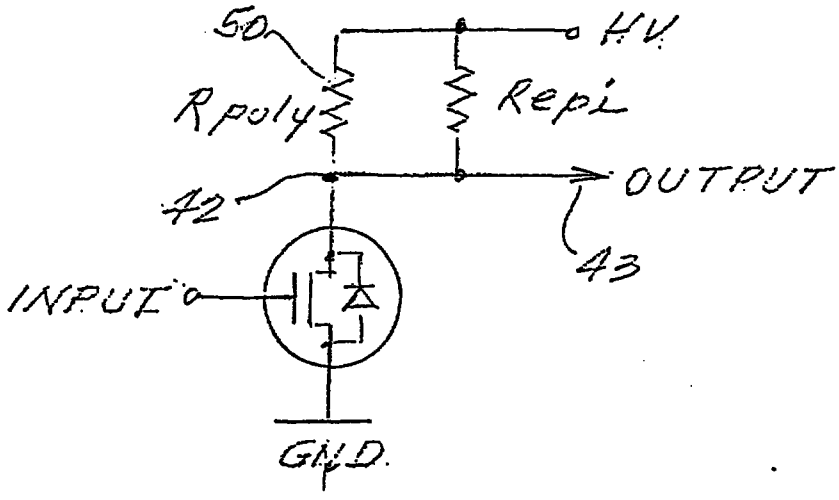


FIG. 6



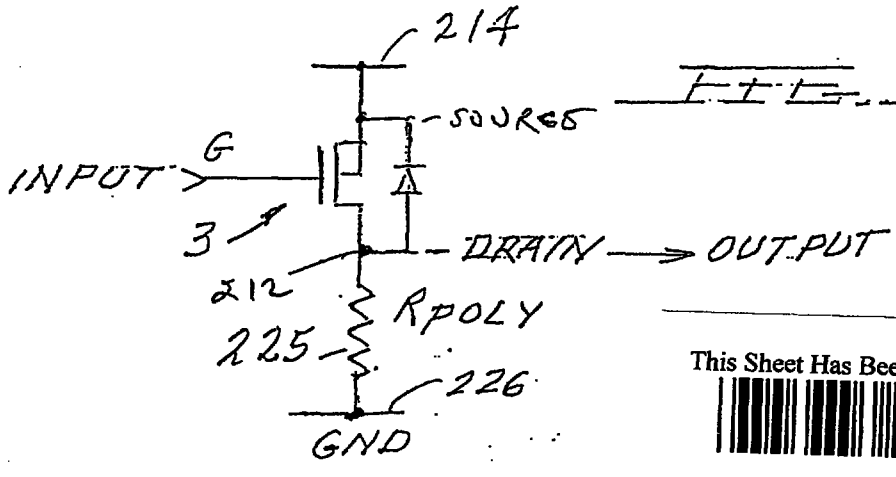


FIG. 9

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FIG. 8

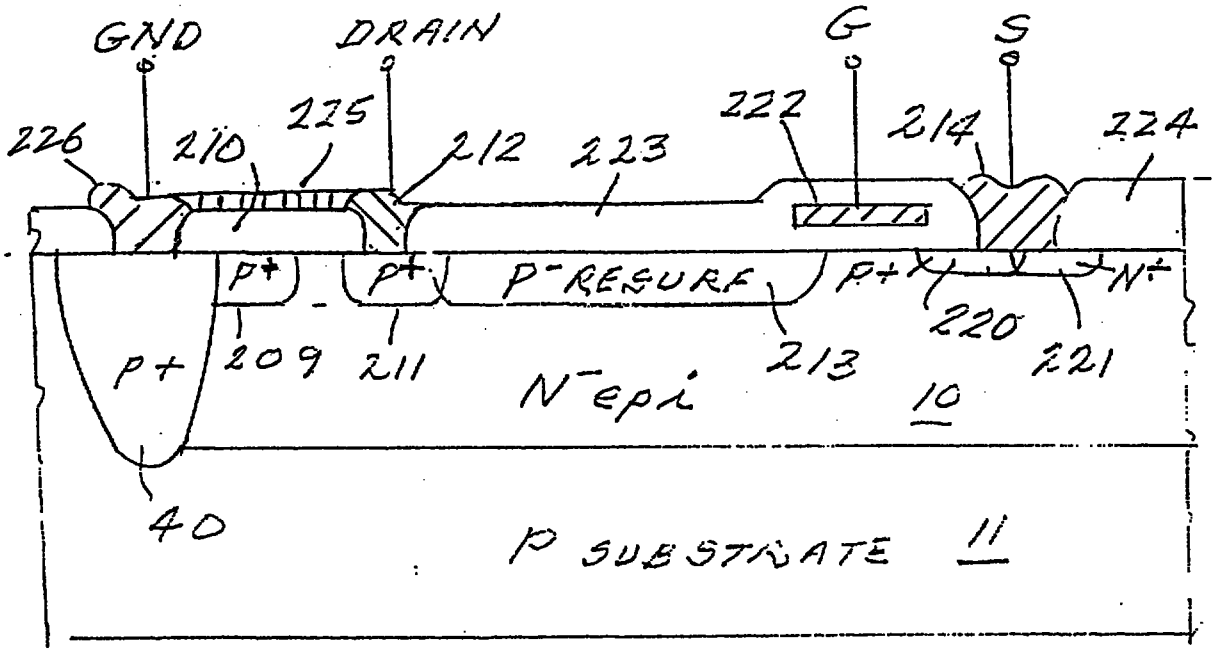
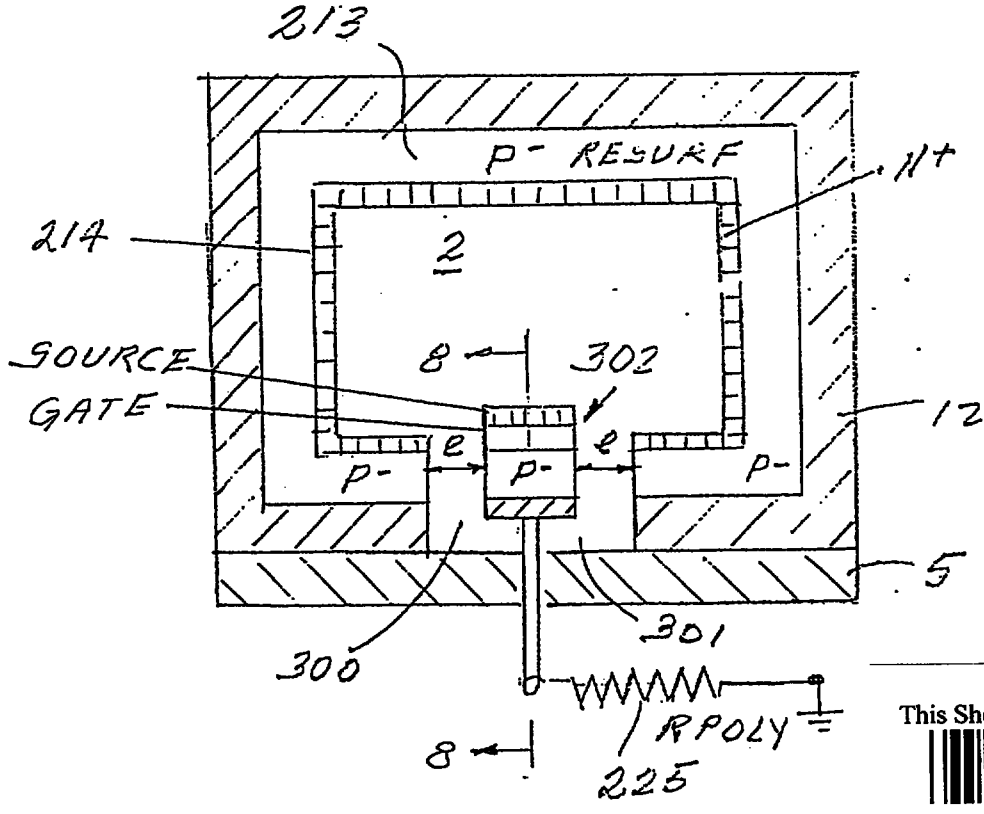


FIG. 13



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FIG. 10

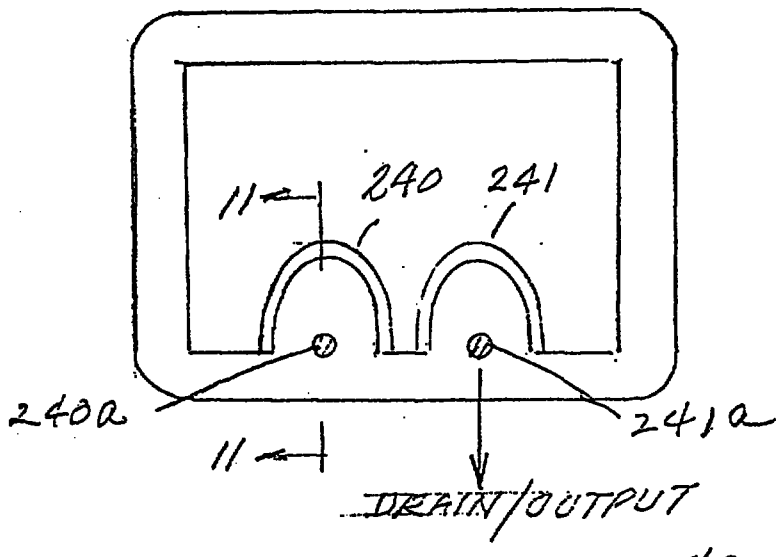


FIG. 11

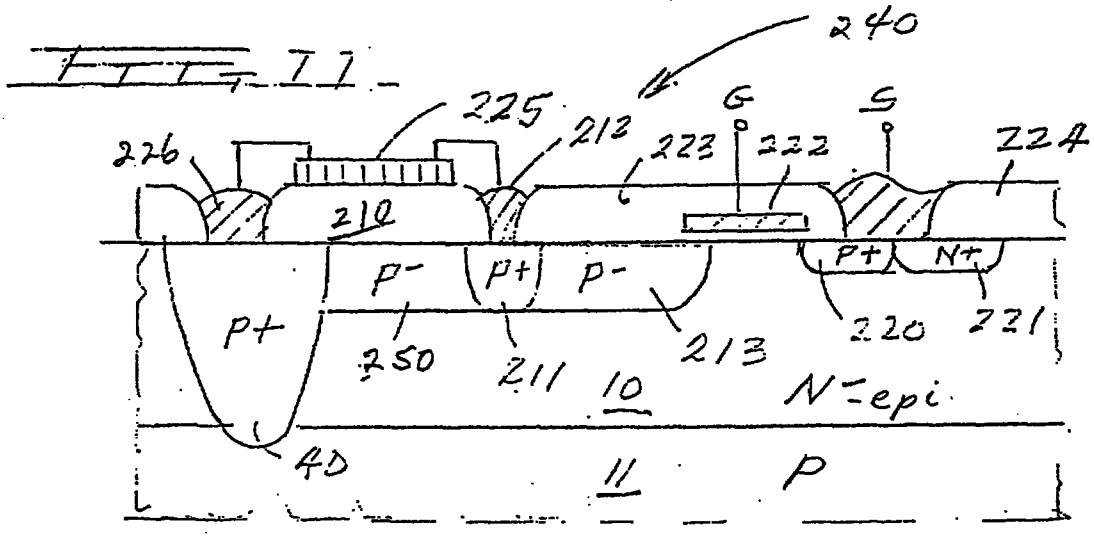
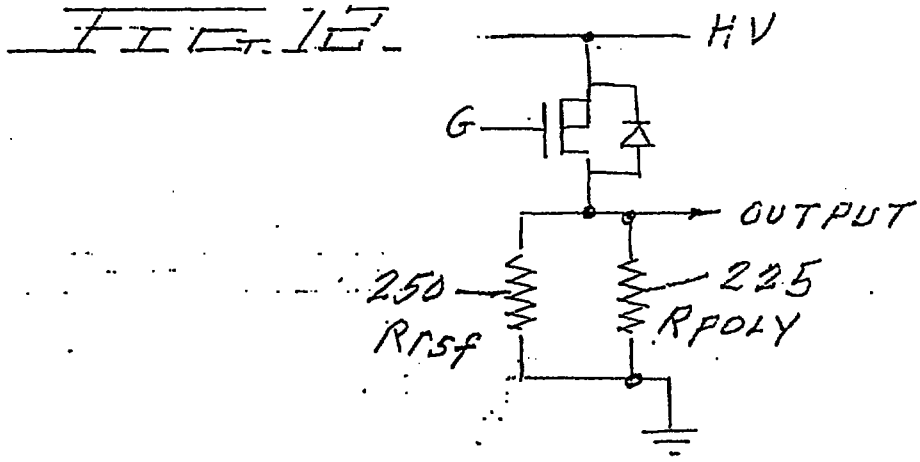


FIG. 12



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FIG. 14

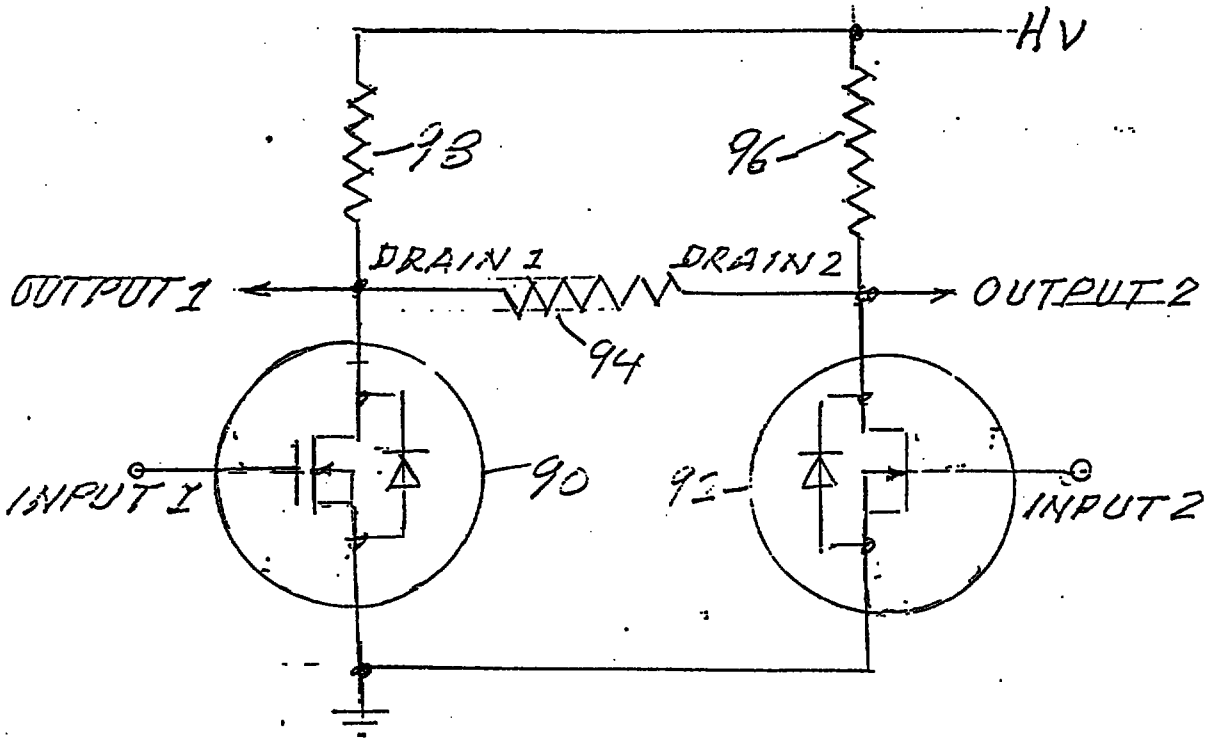
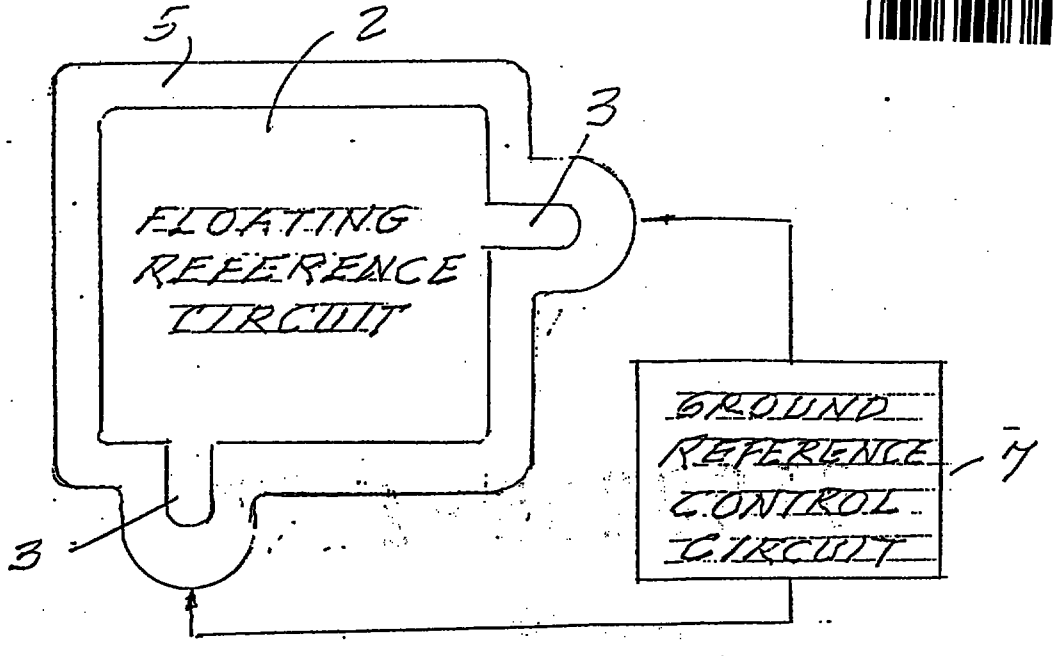


FIG. 15

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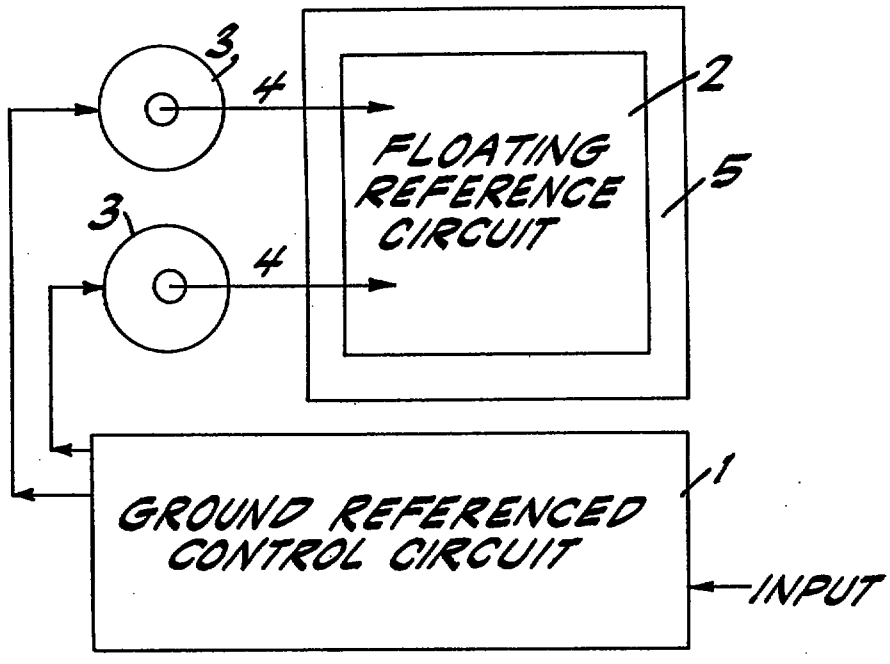
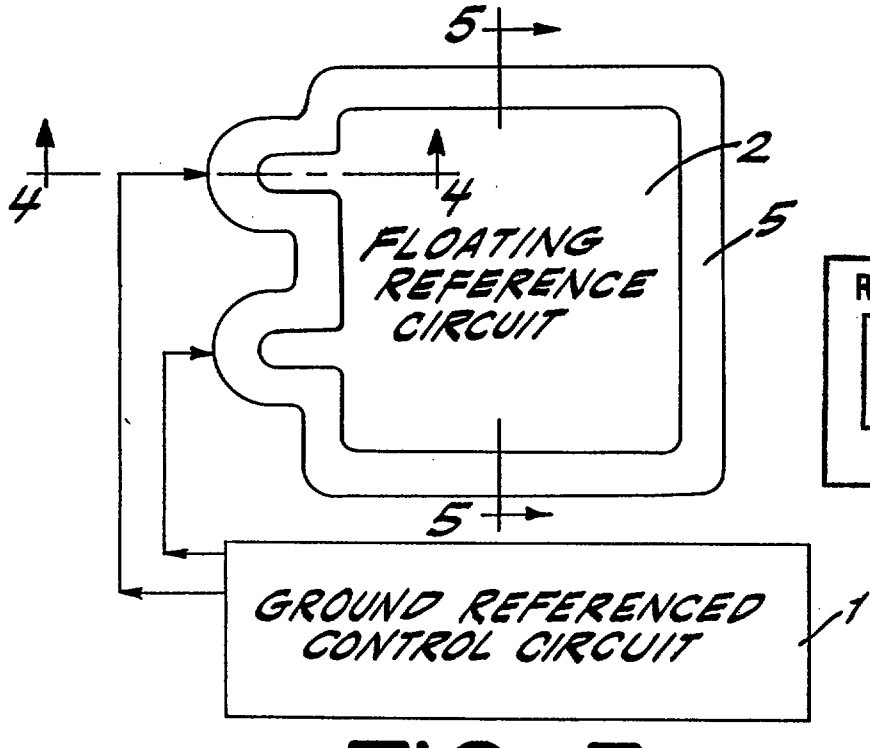


FIG. 1
PRIOR ART



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FIG. 3

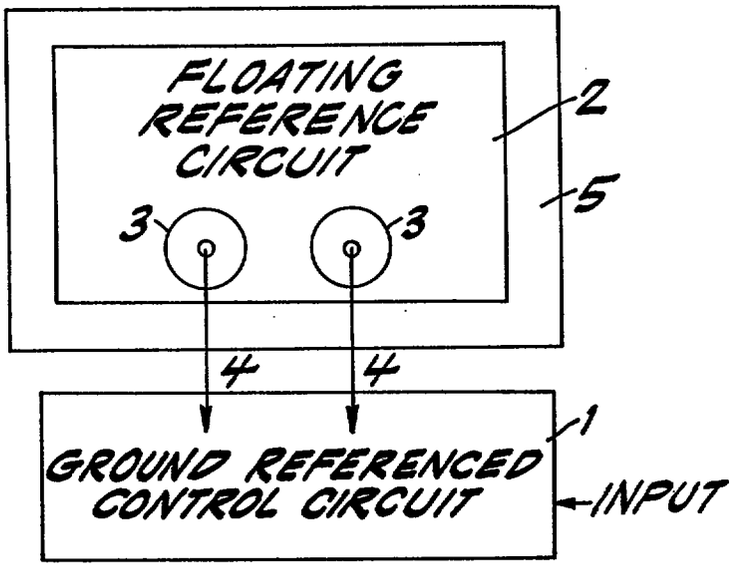


FIG. 2
PRIOR ART

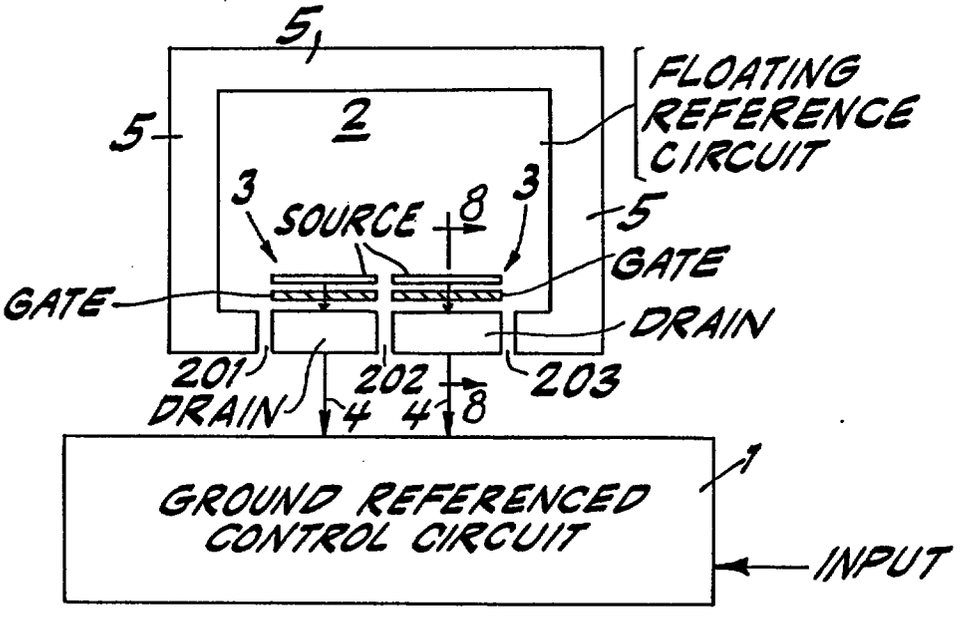


FIG. 7

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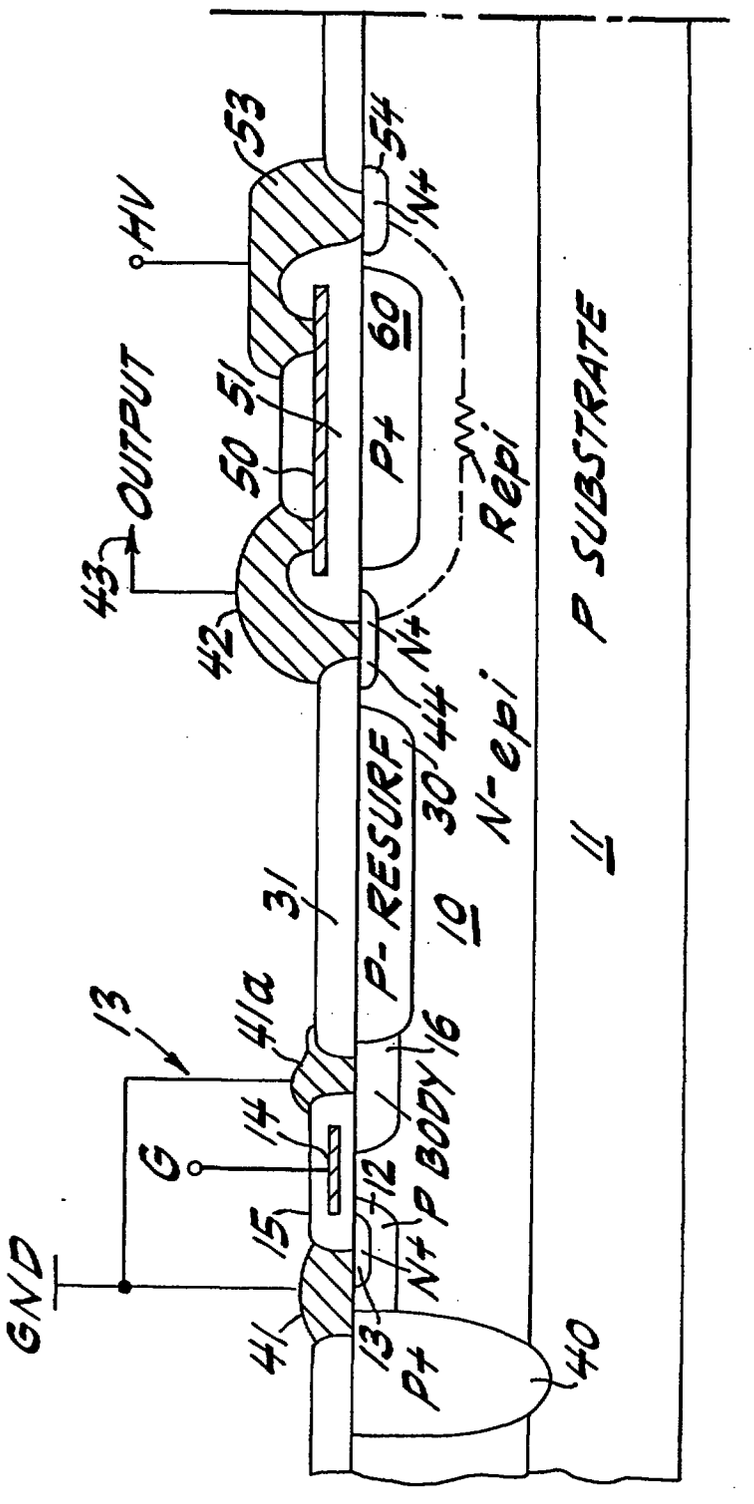


FIG. 4

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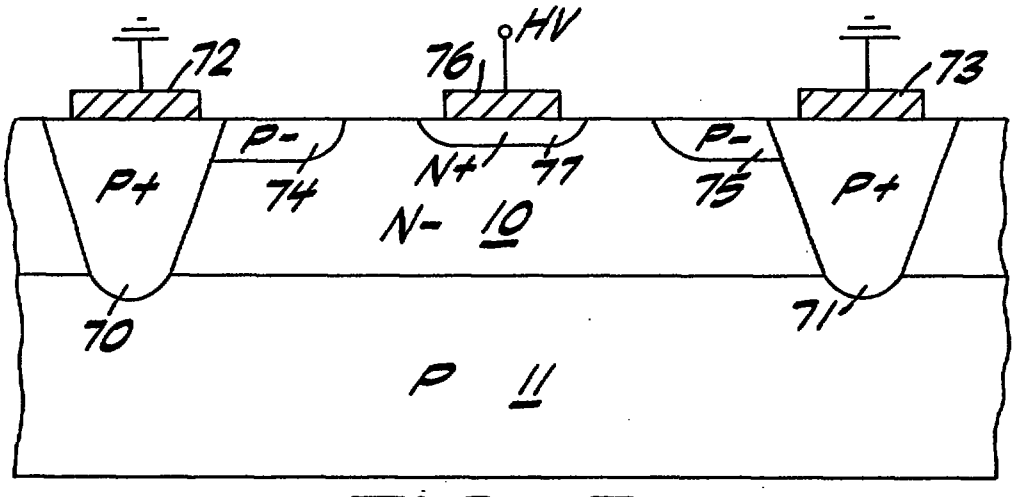


FIG. 5

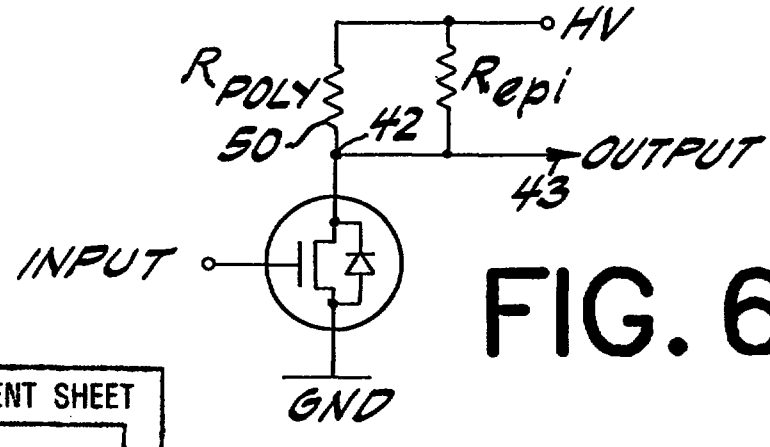


FIG. 6

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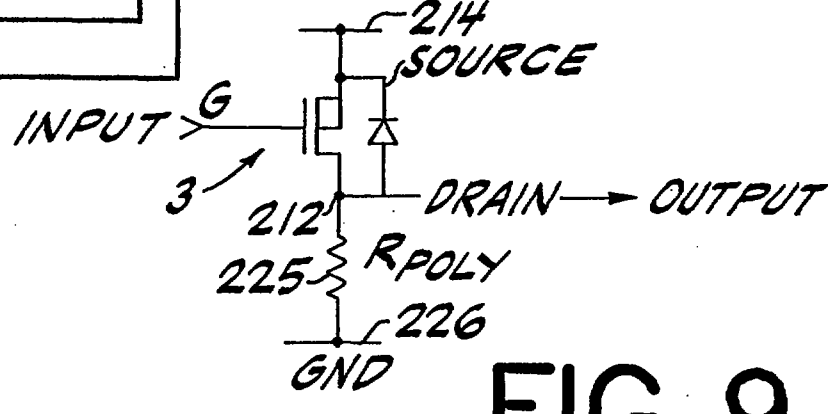


FIG. 9

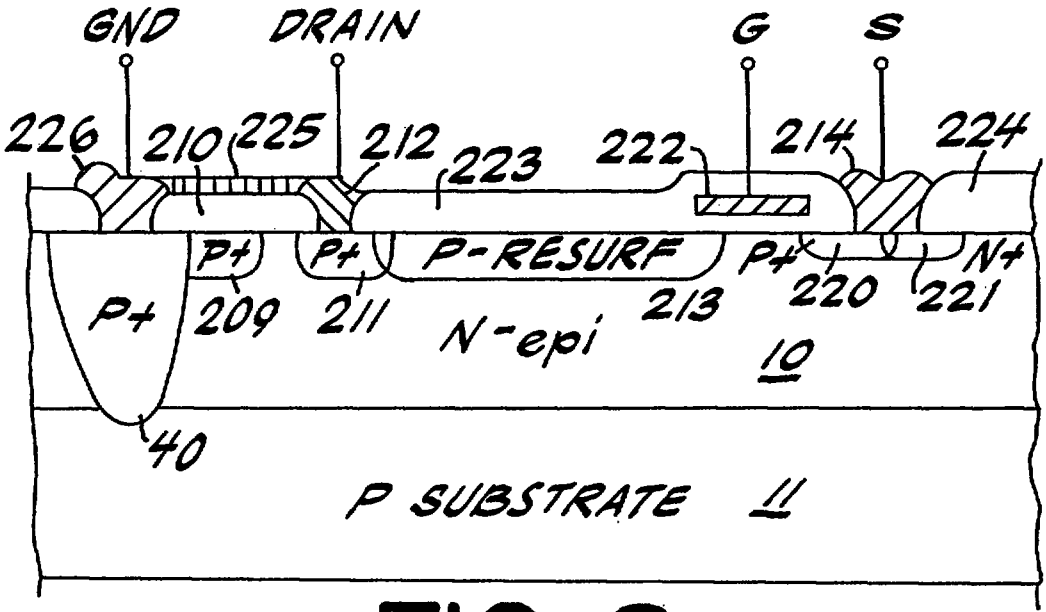


FIG. 8

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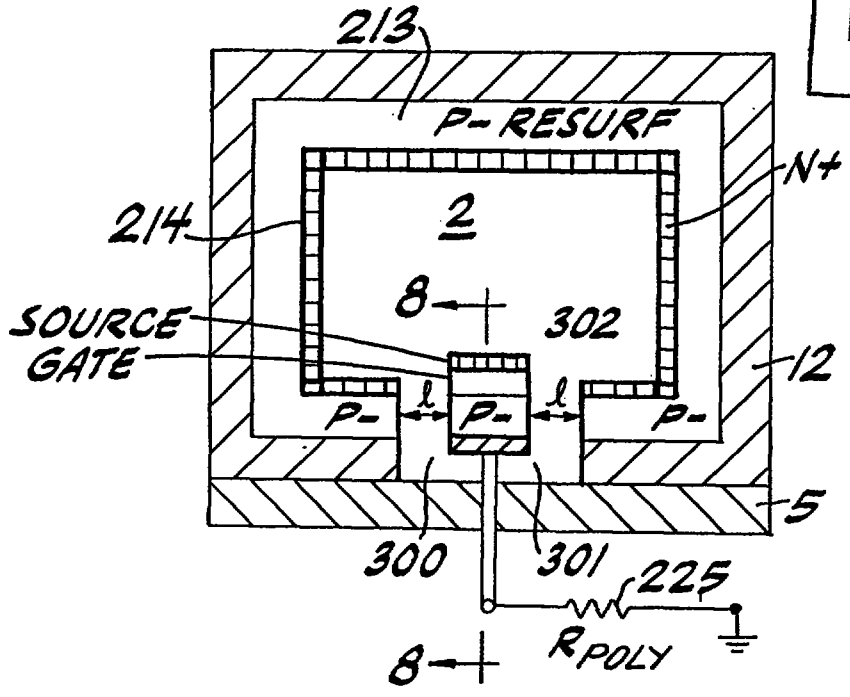


FIG. 13

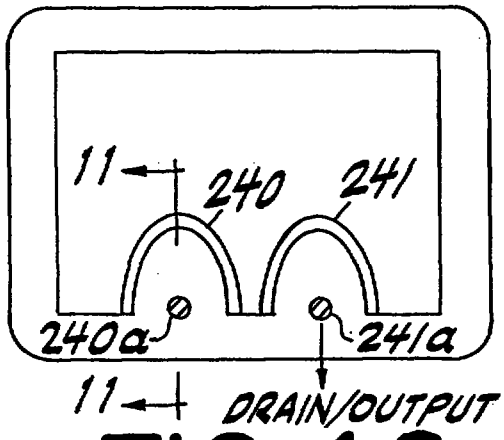


FIG.10

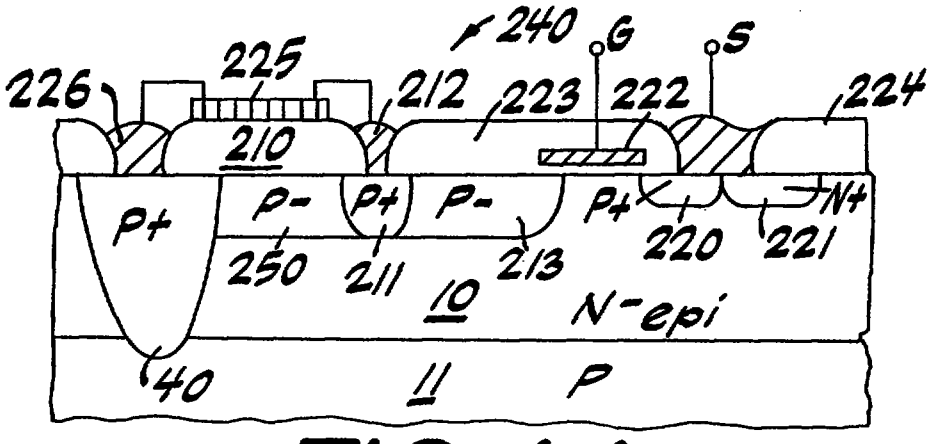


FIG.11

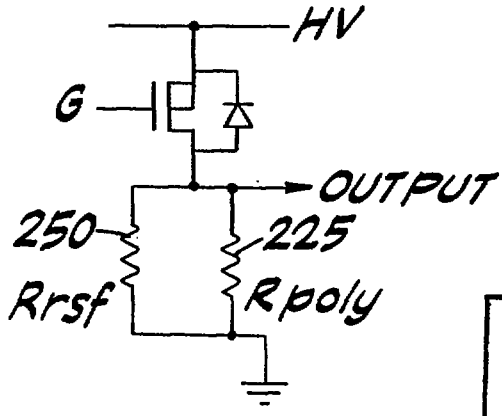


FIG.12

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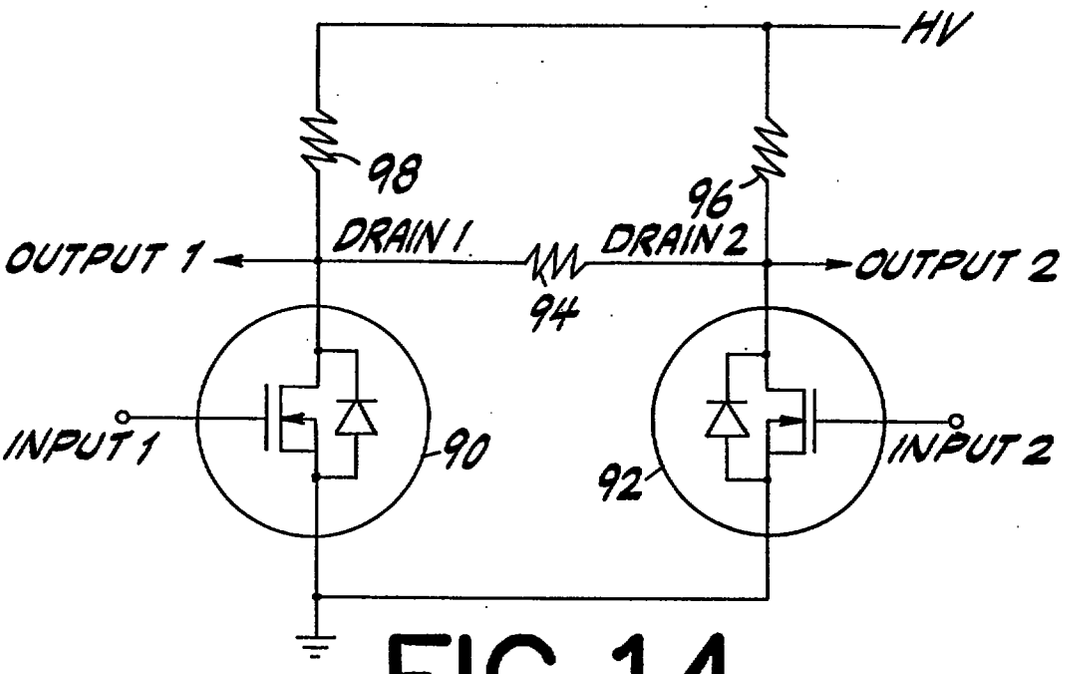


FIG. 14

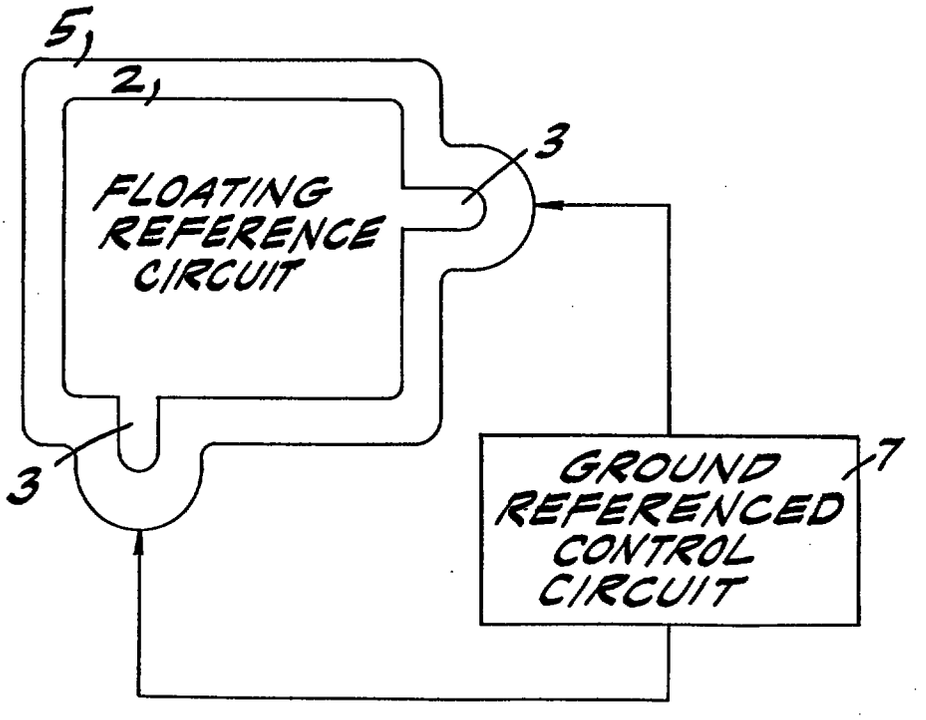


FIG. 15

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☑ Claim(s) : paged 15 to paged 22
☐ Drawing(s) : paged ..... to paged .....
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CLAIMS

1. A level shift device for electrically coupling a floating voltage circuit with a relatively lower voltage circuit each formed on a common substrate (11) of semiconductor material with said level shift circuit, said level shift circuit comprising:

a layer of semiconductor material (10) disposed atop said substrate, said semiconductor material being of a first conductivity type and being lightly doped and having an upper surface;

a base region (12) of a second conductivity type opposite to that of said first conductivity type, said base region extending into the upper surface of said layer of semiconductor material to a given depth and having a substantially semicircular configuration;

a source region (13) of said first conductivity type formed in said base region and defining a surface channel region between said source region and said layer of semiconductor material;

a source electrode (41) connected to said source region and electrically coupled to said lower voltage circuit;

a gate insulation layer disposed over said channel region;

a conductive gate layer (14) disposed over said gate insulation layer;

a drain electrode (42) connected to a portion of said layer of semiconductor material thereby defining a drain region in a portion of said layer of semiconductor material between said channel region and

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said drain electrode, said drain electrode being laterally spaced away from said base region;

a contact electrode (53) connected to another portion of said layer of semiconductor material and electrically coupled to said floating voltage circuit, the portion of said layer of semiconductor material located between said drain electrode and said contact electrode defining a conduction region (R_{cpi}); and

a resistor (50) disposed between said drain electrode and said contact electrode, said resistor being arranged electrically parallel with said conduction region of said layer of semiconductor material.

2. The device of claim 1 wherein said drain region includes a diffusion region (44) of said second conductivity type formed in said upper surface of said layer of semiconductor material to a predetermined depth.

3. The device of claim 1 further comprising another substantially semicircular body region (16) of said second conductivity type formed in said upper surface of said layer of semiconductor material concentric with said base region and disposed between said base region and said drain electrode.

4. The device of claim 3 further comprising a further metal contact (41a) disposed atop at least a portion of said another body region.

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* C L M S *

5. The device of claim 4 wherein said further metal contact is electrically connected to said source electrode.

6. The device of claim 1 further comprising a resurf region (30) of said second conductivity type formed in said upper surface of said layer of semiconductor material and disposed between said another body region and said drain diffusion region and in contact with said another body region.

7. The device of claim 1 wherein said resistor (50) is a conducting layer disposed atop an insulating layer (51).

8. The device of claim 1 further comprising a heavily doped spacer region (40) of said second conductivity type formed in said layer of semiconductor material and extending into the substrate for electrically isolating said device.

9. An integrated circuit comprising a floating voltage circuit (2); a relatively lower voltage circuit (1) ; and a level shift device (3) comprising the device of claims 1, 2, 3, 4, 5, 6, 7 or 8.

10. A device for electrically coupling a floating voltage circuit with a relatively lower voltage circuit each formed in a common substrate (11) with said MOSFET device, said MOSFET device comprising:

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a layer of semiconductor material (10) of first conductivity type disposed atop said substrate and being lightly doped and having an upper surface;

a source diffusion region (220) of said second conductivity type opposite to that of said first conductivity type and formed in said upper surface of said layer of semiconductor material;

a source electrode (214) connected to said source region and electrically coupled to said floating voltage circuit;

a gate insulation layer disposed over a portion of said upper surface of said layer of semiconductor material adjacent to said source diffusion region;

a conductive gate layer (222) disposed over said gate insulation layer;

a drain region (211) of said second conductivity type formed in said upper surface of said layer of semiconductor material and being laterally spaced away from said source diffusion region;

a drain electrode (212) disposed atop said drain diffusion and electrically coupled to said lower voltage circuit; and

a resistor (225) connected between said ground electrode and said drain electrode.

11. The device of claim 10 further comprising a sinker region (40) of said second conductivity type extending from said upper surface of said layer of semiconductor material and extending into said substrate and being laterally spaced away from said drain region

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and being further spaced away from said source diffusion; and

a ground electrode (226) connected to said sinker region.

12. The device of claim 11 further comprising an isolation diffusion region (209) of said second conductivity type formed in said upper surface of said layer of semiconductor material and contacting said sinker region and being laterally spaced away from said drain region to reduce parasitic resistances.

13. The device of claim 10 further comprising a lightly doped resurf region (213) formed in said upper surface of said layer of semiconductor material in contact with said drain region and being arranged between said drain region and said source diffusion region.

14. The device of claim 10 further comprising a further diffusion region (221) of said first conductivity type formed in said upper surface of said layer of semiconductor material and contacting said source diffusion region and said source electrode.

15. An integrated circuit comprising a floating voltage circuit (2) formed in a substrate; a resurf diffusion region (5) substantially surrounding said floating voltage circuit; a relatively lower voltage circuit (1) formed in said substrate; and at least one level shift MOSFET device (3) comprising the device of claims 10, 11, 12, 13 or 14.

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* C L M S *

16. A device for electrically coupling a floating voltage circuit with a relatively lower voltage circuit each formed in a common substrate (10) with said MOSFET device, said MOSFET device comprising:

a layer of semiconductor material of first conductivity type (11) disposed atop said substrate and being lightly doped and having an upper surface;

a source diffusion region (220) of said second conductivity type opposite to that of said first conductivity type, said source diffusion region being formed in said upper surface of said layer of semiconductor material and having a substantially semicircular configuration;

a source electrode (214) connected to said source region and electrically coupled to said floating voltage circuit;

a gate insulation layer disposed over a portion of said upper surface of said layer of semiconductor material adjacent to said source diffusion region;

a conductive gate layer (222) disposed over said gate insulation layer;

a drain region (211) of said second conductivity type formed in said upper surface of said layer of semiconductor material and being laterally spaced away from said source diffusion region;

a drain electrode (212) disposed atop said drain diffusion and electrically coupled to said lower voltage circuit; and

a resistor (225) connected between said ground electrode and said drain electrode.

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17. The device of claim 16 further comprising a sinker region (40) of said second conductivity type extending from said upper surface of said layer of semiconductor material and extending into said substrate and being laterally spaced away from said drain region and being further spaced away from said source diffusion; and

a ground electrode (226) connected to said sinker region.

18. The device of claim 17 further comprising an isolation diffusion region (250) of said second conductivity type formed in said upper surface of said layer of semiconductor material and contacting said sinker region and said drain region.

19. The device of claim 16 further comprising a lightly doped resurf region (213) formed in said upper surface of said layer of semiconductor material in contact with said drain region and being arranged between said drain region and said source diffusion region.

20. The device of claim 16 further comprising a further diffusion region (221) of said first conductivity type formed in said upper surface of said layer of semiconductor material and contacting said source diffusion region and said source electrode.

21. An integrated circuit comprising a floating voltage circuit (2) formed in a substrate; a resurf diffusion region (5) enclosing said high voltage

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circuit; a relatively lower voltage circuit (1) formed in said substrate; and at least one level shift MOSFET device (240, 241) formed in said substrate and electrically coupled between said high voltage circuit and said low voltage circuit, said resurf region at least partially enclosing said level shift MOSFET device and disposed between said level shift MOSFET device and said floating voltage device; said MOSFET device comprising the device of claims 16, 17, 18, 19 or 20.

22. The integrated circuit of claim 21 further comprising a further diffusion region (250) of said second conductivity type formed in said upper surface of said layer of semiconductor material and disposed between and contacting said resurf region and said drain region.

23. The integrated circuit of claim 22 wherein said further diffusion region comprises a further conductive resistor (R_{rsf}) connected between said drain electrode and said ground electrode in parallel with said conductive resistor layer.

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9700257-0

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : C07D 401/04, A61K 31/41, 31/44, 31/495, C07D 249/12 — A1

(11) International Publication Number: WO 96/01818

(43) International Publication Date: 25 January 1996 (25.01.96)

(21) International Application Number: PCT/EP95/02619

(22) International Filing Date: 5 July 1995 (05.07.95)

(30) Priority Data:
94202015.7 12 July 1994 (12.07.94) EP
(34) Countries for which the regional or international application was filed: AT et al.

(71) Applicant *(for all designated States except US)*: JANSSEN PHARMACEUTICA N.V. [BE/BE]; Turnhoutseweg 30, B-2340 Beerse (BE).

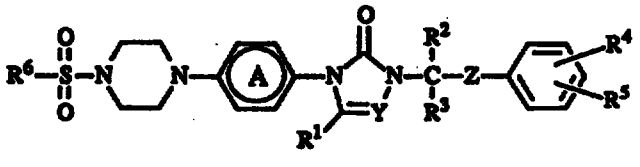
(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: HEERES, Jan [NL/BE]; Leemskuilen 18, B-2350 Vosselaar (BE). STOKBROEKX, Raymond, Antoine [BE/BE]; Rode Kruisstraat 17, B-2340 Beerse (BE). MOSTMANS, Joseph, Hector [BE/BE]; Breughelstraat 28 bus 3, B-2018 Antwerpen (BE). VAN DER VEKEN, Louis, Jozef, Elisabeth [BE/BE]; Oudebaan 48, B-2350 Vosselaar (BE).

(81) Designated States: AM, AU, BB, BG, BR, BY, CA, CN, CZ, EE, FI, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LT, LV, MD, MG, MN, MW, MX, NO, NZ, PL, RO, RU, SD, SG, SI, SK, TJ, TT, UA, UG, US, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, MW, SD, SZ, UG).

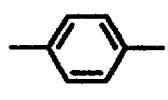
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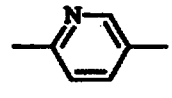
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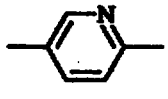
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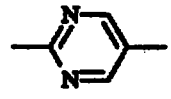


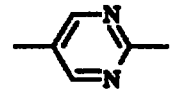


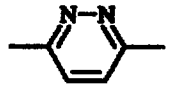


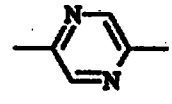












(57) Abstract

The invention is concerned with the compounds having formula (I) the pharmaceutically acceptable addition salts and the stereochemically isomeric forms thereof, wherein Y is CH or N; R^1, R^2 and R^3 each independently are hydrogen or C_{1-4}alkyl; R^4 and R^5 each independently are hydrogen, halo, C_{1-4}alkyl, C_{1-4}alkyloxy, hydroxy, trifluoromethyl, trifluoromethyloxy or difluoromethyloxy; R^6 is C_{1-4}alkyl; or phenyl optionally substituted with halo, C_{1-4}alkylcarbonylamino, C_{1-4}alkyloxy, C_{1-4}alkyl or nitro; Z is C=O or CHOH; and (1) is a radical of formula ((a-1), (a-2), (a-3), (a-4), (a-5), (a-6), or (a-7). Compositions comprising said compounds, processes for preparing the same and the use of these compounds as a medicine.

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