ABSTRACT

METHOD OF FABRICATING WEDGE ISOLATION TRANSISTORS

A method of fabricating a transistor, comprising the following steps. A silicon semiconductor structure having spaced, raised, wedge-shaped dielectric isolation regions defining an active region there between is provided. Epitaxial silicon is grown over the active area to form an SEG region. A dummy gate is formed over the SEG region. Raised epitaxial silicon layers are grown over the SEG region adjacent the dummy gate. The dummy gate is removed, exposing the interior side walls of the raised epitaxial silicon layers. Sidewall spacers are formed on the exposed sidewalls of the raised epitaxial silicon layers. A gate oxide layer is grown over the SEG region and between the sidewall spacers of the raised epitaxial silicon layers. A layer of polysilicon is deposited over the structure and is planarized to form a gate conductor over the SEG region and between the sidewall spacers of the raised epitaxial silicon layers. The sidewall spacers are removed. No HDP process trench fill is required to form the STIs and no CMP process is required to planarized the STIs.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)