METHOD OF MANUFACTURING A SEMICONDUCTOR HETEROSTRUCTURE

ABSTRACT

The invention relates to a method of manufacturing a semiconductor heterostructure, comprising manufacturing a donor wafer, comprising providing a first substrate with a first in-plane lattice parameter, providing on the first substrate a spatially graded buffer layer having on top in a relaxed state a second in-plane lattice parameter, forming on the graded buffer layer an ungraded layer of a semiconductor material having in a relaxed state a third in-plane lattice parameter, forming on the ungraded layer a top layer of a semiconductor material, and manufacturing a handle wafer, comprising providing a second substrate, forming on the second substrate an insulator layer, and bonding the donor wafer with the handle wafer. It is the object of the invention to reduce the thermal load on the donor wafer substrate with the top layer before bonding and to achieve nevertheless good bonding results. The object is solved by a method of the above mentioned type according to which said ungraded layer is a strained smoothing layer wherein the third in-plane lattice parameter of this strained smoothing layer is between the first and second lattice parameter, and said handle wafer is bonded with the donor wafer in such way that the insulator layer of the handle wafer is bonded directly onto the free surface of the top layer of the donor wafer, or the insulator layer of the handle wafer is bonded onto a superficial layer being present on the surface of the top layer of the donor wafer, said superficial layer having a thickness being equal to or smaller than 10 nanometres.

Fig. 1a –1g