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ETCH/CLEAN PROCESS FOR INTEGRATED CIRCUIT PAD METAL

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to a method of etching an opening to metal bonding pads, and more particularly, to a method of etching an opening to metal bonding pads where corrosion and fluorine contamination of the metal bonding pads is reduced in the manufacture of integrated circuits.

(2) Description of the Prior Art

In the fabrication of integrated circuits, various semiconductor devices and interconnections are fabricated in multiple layers on a semiconductor substrate. The final metallization layer includes bonding pads which are typically located on the periphery of the integrated circuit. The integrated circuit chip's external wiring is bonded to these metal bonding pads. Before this external wiring is connected, the metal bonding pads underlying a passivation layer must be exposed with a contact etch through the passivation layer and subsequent cleaning steps to remove photoresist residues and etch polymers.

The etch and clean steps significantly degrade the quality of the aluminum pad metal. The etch process causes fluorine contamination of the aluminum which interferes with aluminum oxide growth as well as causing high resistance during wafer probe and yield variability. The clean steps cause and accelerate galvanic corrosion of the aluminum pad metal at grain boundaries where copper precipitates exist. The galvanic corrosion creates pits in the metal surface. These pits will grow and propagate through the aluminum layer as the corrosion proceeds, a significant issue for wafer storage. The corrosion is a quality and reliability problem for both wire bonded and bumped pads.

Workers in the art have sought to avoid or reduce the problems of chlorine or fluorine contamination and corrosion. U.S. Patent 5,376,235 to Langley teaches cleaning the metal bonding pad after etching with a solution of de-ionized water and phosphoric acid to remove fluorine residue. U.S. Patent 5,930,664 to Hsu et al teaches a method of first etching the passivation layer, then etching through the ARC layer, then forming a polymer over the metal bonding pad for protection. U.S. Patent 6,001,538 to Chen et al discloses a two-step etching process to form an opening to a bonding pad. U.S. Patent 5,540,812 to Kadomura shows an

aluminum etching process using various methods to prevent corrosion caused by chlorine contamination.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of etching an opening to a bonding pad.

Another object of the present invention is to provide a method of etching an opening to a bonding pad wherein corrosion is eliminated.

A further object of the present invention is to provide a method of etching an opening to a bonding pad wherein corrosion is eliminated and fluorine contamination is reduced.

Yet another object of the present invention is to provide a method of etching an opening to a bonding pad wherein corrosion is eliminated and fluorine contamination is reduced by adding a hard mask protective layer over the passivation layer and by removing the anti-reflective coating layer over the bonding pad after all other etching and cleaning has been completed.

In accordance with the objects of this invention a new method of etching an opening to a bonding pad wherein corrosion is eliminated and fluorine contamination is reduced is achieved. A metal bonding pad is provided overlying an insulating layer on a semiconductor substrate. An anti-reflective coating (ARC) layer is deposited overlying the metal bonding pad. A passivation layer is deposited overlying the ARC layer. A hard mask layer is deposited overlying the passivation layer. A photoresist mask is formed overlying the hard mask layer having an opening where the contact opening to the metal bonding pad is to be made. The hard mask layer and passivation layer not covered by the photoresist mask are etched through, stopping at the ARC layer. Thereafter, the photoresist mask is removed and the opening is cleaned. The ARC layer protects the metal bonding pad during these steps. The ARC layer within the opening is etched away wherein the hard mask layer overlying the passivation layer prevents erosion of the passivation layer thereby preventing contamination of the metal bonding pad to complete opening a contact to a metal bonding pad in the fabrication of an integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 6 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The novel method of forming a contact to a metal bonding pad where corrosion is eliminated and fluorine contamination is reduced will be described with reference to the drawing figures. It will be understood by those skilled in the art that the process of the invention should not be limited to the embodiment shown herein, but can be applied and extended to other various materials and applications.

Referring now more particularly to Fig. 1, there is illustrated a portion of a partially completed integrated circuit. Semiconductor substrate 10 is preferably composed of monocrystalline silicon. Semiconductor device structures, such as gate electrodes and associated source and drain regions and multiple levels of interconnection lines,

not shown, are fabricated in and on the semiconductor substrate. These underlying devices and layers are included in the layer labeled 14 in Fig. 1. An insulating layer within 14 covers the underlying layers.

Now, the topmost metal layer is to be formed. The bonding pads will be formed in this topmost metal layer. The present invention is a process flow for etching an opening to the metal bonding pad and cleaning the opening so as to eliminate pad pitting, caused by corrosion, and significantly to reduce fluorine contamination that results from etching and cleaning. This will improve significantly the quality of the metal pad. Reducing the fluorine content on the surface of the pad metal results in a higher quality pad metal surface with improved native oxide uniformity which is highly desirable for improved yield at wafer probe, improved yield in solder bump processing, and extended wafer storage.

The metal layer 20, typically aluminum or aluminum with copper and/or silicon is deposited over the topmost insulating layer in layer 14. A barrier layer, not shown, may be deposited underlying the metal layer 20. The aluminum layer 20 is deposited by sputtering or chemical vapor deposition (CVD) to a thickness of between about 5000

and 18,000 Angstroms. An antireflective coating (ARC) layer 22 of titanium nitride, titanium tungsten, or one of several organic or inorganic ARC materials is deposited overlying the metal layer 20 to a thickness of between about 100 and 500 Angstroms.

Now, a passivation layer 26 is deposited over the ARC layer 22. The passivation layer may comprise silicon nitride or a combination of high density plasma (HDP) silicon oxide and silicon nitride or tetreaethoxysilane (TEOS) oxide. The passivation layer typically has a thickness of between about 5000 and 20,000 Angstroms.

Now, the novel process steps of the present invention will be described. Referring now to Fig. 2, a hard mask layer 30 is deposited over the passivation layer. This hard mask layer may comprise titanium nitride, titanium tungsten, or one of several organic or inorganic ARC materials commonly used in the industry and have a thickness of between about 100 and 500 Angstroms. The hard mask layer may or may not comprise the same material as the ARC layer 22.

Referring now to Fig. 3, a layer of photoresist is coated over the hard mask layer 30 and is

exposed and developed to form the photoresist mask 35, having an opening where the contact to the metal bonding pad is to be made.

Now, a plasma etch is performed to etch through the hard mask layer 30 and the passivation layer 26, stopping at the buried ARC layer 22, as shown in Fig. 4. For example, a low pressure plasma etch may be employed, typically at 350 mTorr pressure with an etch environment comprising CHF_3, CF_4, and argon gases, proportioned by flow rate, typically 10 sccm CHF_3, 70 sccm CF_4, and 900 sccm Ar. The etch is either timed to stop on the underlying ARC layer or stopped by endpoint detection means commonly used in the industry.

The ARC layer 22 serves as a protective film over the metal surface, preventing fluorine contamination and corrosion pitting during the passivation etch.

The photoresist mask is stripped using, for example, O_2/CF_4 plasma ashing, as shown in Fig. 5. This step is followed by a cleaning step to remove resist residues and etch polymers. The cleaning step may comprise a wet chemistry organic solvent; for example, EKC265 for 10 minutes, followed by isopropyl alcohol (IPA) for 400 seconds,

followed by a de-ionized water rinse with CO_2 agitant for 390 seconds. Alternatively, a developer clean, such as Tetra-Methyl-Ammonium-Hydroxide (TMAH) may be used for 10 to 60 seconds. The ARC layer also provides protection for the metal layer during the photoresist stripping and wet cleans.

After the clean step, a second plasma etch is performed to remove the ARC layer 22 within the opening. When the underlying ARC layer comprises titanium nitride, the same chemistry etch recipe is used as described above for the first plasma etch step with end point detection on the aluminum pad metal. Fluorine chemistry is not necessary in this case.

For the preferred embodiment, which teaches titanium nitride as the hard mask, it is necessary that the second plasma etch completely remove both the underlying ARC layer 22 and the hard mask layer 30 simultaneously, as shown in Fig. 6. However, this requirement does not necessarily apply to other materials that can serve as the hard mask. In some cases, it may be desirable to leave some of all of the hard mask behind after complete etch of the underlying ARC film exposing the metal surface.

In either case, the hard mask layer 30 prevents erosion of the passivation layer during etching away of the ARC layer 22. Silicon nitride passivation has approximately a 10:1 higher etch rate than does titanium nitride, so significant erosion would occur if the passivation layer were not protected by the hard mask layer during etching.

Now, the metal bonding pad exposed within the contact opening may be alloyed as usual and processing continues to make connections to the bonding pad, such as by wire bonding, solder bump processing, or the like, not shown.

The process of the present invention provides an effective method for opening a contact to a metal bonding pad wherein pad pitting is eliminated and fluorine contamination is greatly reduced. Adding a hard mask layer over the passivation layer and retaining the ARC layer over the metal bonding pad until just before alloying achieves the high quality metal bonding pad of the present invention.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be

made without departing from the spirit and scope of the invention.

What is claimed is :

1. A method of opening a contact to a metal bonding pad in the fabrication of an integrated circuit comprising:

providing a metal bonding pad overlying an insulating layer on a semiconductor substrate;

depositing an anti-reflective coating (ARC) layer overlying said metal bonding pad;

depositing a passivation layer overlying said ARC layer;

depositing a hard mask layer overlying said passivation layer;

forming a photoresist mask overlying said hard mask layer having an opening where said contact opening to said metal bonding pad is to be made;

etching through said hard mask layer and said passivation layer not covered by said photoresist mask and stopping at said ARC layer;

thereafter removing said photoresist mask and cleaning said opening wherein said ARC layer protects said metal bonding pad; and

thereafter etching away said ARC layer within said opening wherein said hard mask layer overlying said passivation layer prevents erosion of said passivation layer thereby preventing contamination of said metal bonding pad to complete opening said contact to said metal bonding pad in said fabrication of said integrated

circuit.

2. The method according to Claim 1 wherein said semiconductor substrate includes semiconductor device structures such as gate electrodes, source and drain regions, and interconnection lines underlying said insulating layer.

3. The method according to Claim 1 wherein said metal bonding pad comprises aluminum.

4. The method according to Claim 1 wherein said metal bonding pad comprises one of the group containing aluminum, aluminum-copper, aluminum-silicon, and aluminum-copper-silicon.

5. The method according to Claim 1 further comprising depositing a barrier metal layer underlying said metal bonding pad.

6. The method according to Claim 1 wherein said ARC layer comprises one of the group containing: titanium nitride, titanium tungsten, organic ARC materials, and inorganic ARC materials and has a thickness of between about 100 and 500 Angstroms.

7. The method according to Claim 1 wherein said passivation layer comprises silicon nitride having a thickness of between about 5000 and 20,000 Angstroms.

8. The method according to Claim 1 wherein said passivation layer comprises high density plasma oxide and silicon nitride having a combined thickness of between about 5000 and 20,000 Angstroms.

9. The method according to Claim 1 wherein said hard mask layer comprises titanium nitride, titanium tungsten, and organic ARC materials and has a thickness of between about 100 and 500 Angstroms.

10. The method according to Claim 1 wherein said step of etching through said hard mask layer and said passivation layer comprises a plasma etch using CHF_3, CF_4, and Ar chemistry.

11. The method according to Claim 1 wherein said step of removing said photoresist mask comprises stripping said photoresist mask using O_2/CF_4 plasma ashing.

12. The method according to Claim 1 wherein said step of cleaning said opening comprises a wet chemistry organic

solvent, isopropyl alcohol, and de-ionized water rinse.

13. The method according to Claim 1 wherein said step of etching away said ARC layer within said opening comprises a plasma etch using CHF_3, CF_4, and Ar chemistry.

14. The method according to Claim 1 wherein said step of etching away said ARC layer within said opening simultaneously etches away said hard mask layer overlying said passivation layer.

15. A method of opening a contact to a metal bonding pad in the fabrication of an integrated circuit comprising:

providing semiconductor devices structures in and on a semiconductor substrate wherein said semiconductor device structures are covered by an insulating layer;

depositing a metal bonding pad overlying said insulating layer;

depositing an anti-reflective coating (ARC) layer overlying said metal bonding pad;

depositing a passivation layer overlying said ARC layer;

depositing a hard mask layer overlying said passivation layer;

forming a photoresist mask overlying said hard mask layer having an opening where said contact opening to said metal bonding pad is to be made;

etching through said hard mask layer and said passivation layer not covered by said photoresist mask and stopping at said ARC layer;

thereafter removing said photoresist mask and cleaning said opening wherein said ARC layer protects said metal bonding pad; and

thereafter etching away said ARC layer within said opening wherein said hard mask layer overlying said passivation layer prevents erosion of said passivation layer thereby preventing contamination of said metal bonding pad to complete opening said contact to said metal bonding pad in said fabrication of said integrated circuit.

16. The method according to Claim 15 wherein said semiconductor device structures comprise gate electrodes, source and drain regions, and interconnection lines.

17. The method according to Claim 15 wherein said metal bonding pad comprises one of the group containing

aluminum, aluminum-copper, aluminum-silicon, and aluminum-copper-silicon.

18. The method according to Claim 15 further comprising depositing a barrier metal layer underlying said metal bonding pad.

19. The method according to Claim 15 wherein said ARC layer comprises titanium nitride, titanium tungsten, organic ARC materials, and inorganic ARC materials and has a thickness of between about 100 and 500 Angstroms.

20. The method according to Claim 15 wherein said passivation layer comprises silicon nitride having a thickness of between about 5000 and 20,000 Angstroms.

21. The method according to Claim 15 wherein said passivation layer comprises high density plasma oxide and silicon nitride having a combined thickness of between about 5000 and 20,000 Angstroms.

22. The method according to Claim 15 wherein said hard mask layer comprises titanium nitride, titanium tungsten, and organic ARC materials and has a thickness of between about 100 and 500 Angstroms.

23. The method according to Claim 15 wherein said step of etching through said hard mask layer and said passivation layer comprises a plasma etch using CHF_3, CF_4, and Ar chemistry.

24. The method according to Claim 15 wherein said step of removing said photoresist mask comprises stripping said photoresist mask using O_2/CF_4 plasma ashing.

25. The method according to Claim 15 wherein said step of cleaning said opening comprises a wet chemistry organic solvent, isopropyl alcohol, and de-ionized water rinse.

26. The method according to Claim 15 wherein said step of etching away said ARC layer within said opening comprises a plasma etch using CHF_3, CF_4, and Ar chemistry.

27. The method according to Claim 15 wherein said step of etching away said ARC layer within said opening simultaneously etches away said hard mask layer overlying said passivation layer.

28. A method of opening a contact to an aluminum bonding pad in the fabrication of an integrated circuit comprising:

providing semiconductor devices structures in and on a semiconductor substrate wherein said semiconductor device structures are covered by an insulating layer;

depositing a aluminum bonding pad overlying said insulating layer;

depositing an anti-reflective coating (ARC) layer overlying said aluminum bonding pad;

depositing a silicon nitride passivation layer overlying said ARC layer;

depositing a titanium nitride layer overlying said passivation layer;

forming a photoresist mask overlying said titanium nitride layer having an opening where said contact opening to said aluminum bonding pad is to be made;

etching through said titanium nitride layer and said passivation layer not covered by said photoresist mask and stopping at said ARC layer;

thereafter removing said photoresist mask and cleaning said opening wherein said ARC layer protects said aluminum bonding pad; and

thereafter etching away said ARC layer within said opening wherein said titanium nitride layer overlying

said passivation layer prevents erosion of said passivation layer thereby preventing contamination of said aluminum bonding pad to complete opening said contact to said aluminum bonding pad in said fabrication of said integrated circuit.

29. The method according to Claim 28 wherein said semiconductor device structures comprise gate electrodes, source and drain regions, and interconnection lines.

30. The method according to Claim 28 wherein said ARC layer comprises titanium nitride having a thickness of between about 100 and 500 Angstroms.

31. The method according to Claim 28 wherein said step of etching through said titanium nitride layer and said passivation layer comprises a plasma etch using CHF_3, CF_4, and Ar chemistry.

32. The method according to Claim 28 wherein said step of removing said photoresist mask comprises stripping said photoresist mask using O_2/CF_4 plasma ashing.

33. The method according to Claim 28 wherein said step of cleaning said opening comprises a wet chemistry organic solvent, isopropyl alcohol, and de-ionized water rinse.

34. The method according to Claim 28 wherein said step of etching away said ARC layer within said opening comprises a plasma etch using CHF_3, CF_4, and Ar chemistry.

35. The method according to Claim 28 wherein said step of etching away said ARC layer within said opening simultaneously etches away said titanium nitride layer overlying said passivation layer.