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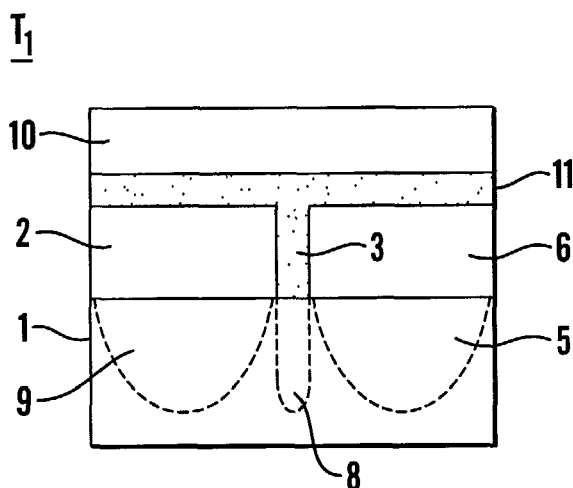
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(54) Title: A MATRIX-ADDRESSABLE ARRAY OF INTEGRATED TRANSISTOR/MEMORY STRUCTURES



(57) Abstract: comprises one or more layers (1) of semiconducting material, two or more electrode layers, and memory material (11) contacting electrodes (2, 6, 10) in the latter. At least one layer of a semiconducting material and two electrode layers form transistor structures such that the electrodes of the first electrode layer forms source/drain electrode pairs and those of a second electrode layer form the gate electrodes thereof. The source and drain electrodes (2, 6) of a single transistor/memory structure are separated by a narrow recess (3) extending down to the semiconducting (1) layer wherein the transistor channel (8) is provided beneath the recess and with extremely small width, while the source and drain regions are provided beneath the respective source and drain electrodes (2, 6) on either side of the transistor channel (8). Memory material (11) is provided in the recess (3) and contacts the electrodes (2, 6, 10) of the transistor. This arrangement defines the transistor channel (8) with a length L corresponding to the width of the recess (3) and a width W corresponding to the width of the gate electrode (10), L being

a fraction of W, and three memory cells in the memory material (11) formed respectively between the source electrode (2) and the gate electrode (10), the drain electrode (6) and the gate electrode (10) and in the recess between the source and drain electrodes (2, 6).

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