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(54) IMPROVEMENTS IN OR RELATING TO GATE CONTROL APPARATUS

(71) We, HEWLETT - PACKARD COMPANY, of 1501 Page Mill Road, Palo Alto, California, United States of America, a corporation organised and existing under the laws of the state of California, United States of America, do hereby declare this invention, for which we pray that a Patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention is concerned with improvements in or relating to gate control apparatus. Certain known frequency measuring devices convert an input signal having an unknown frequency into uniform pulses. Frequency measurements are made by routing these pulses through a main gate and into a decade counting assembly where the pulses are totalized. The number of pulses totalized during the time interval for which the main gate is open is a measure of the average frequency of the input signal for that time interval. A time base selector switch is manually operated to select a time interval, position the decimal point and select the appropriate measurement unit.

An error of $+1$ count may be introduced into the measurement when the opening and closing of the main gate is unsynchronized with the input signal. The fractional effect of this error is $1/(\text{total events counted})$ and therefore greater accuracy is achieved with longer time intervals.

One disadvantage of known frequency measuring devices is that the time interval (commonly referred to as the gate time) must be established prior to the initiation of a measurement. A gate time is selected and a measurement is initiated. If the input frequency is too high for that gate time, the decade counting assembly may overflow and another measurement at a shorter gate time may be needed. If the input frequency is too low for that gate time the accuracy and resolution of the measurement may be so poor that another measurement at a longer gate time may be needed. A similar problem is

found in certain multiperiod averaging devices that require an operator to determine the number of periods of an input signal to average, prior to the initiation of a measurement.

The time base apparatus of certain known frequency measuring devices comprises a reference frequency source and a decade divider assembly. One disadvantage of this type of time base apparatus is that the decade divider has a separate output line for each separate gate time. The time base selector switch aforementioned selects which of these outputs is to be used to provide the gate time. This provides a significant problem when it is desired to have available a number of gate times and when the time base apparatus is being made as an integrated circuit.

It is an object of the present invention to provide improved selective timing means.

It is another object of the present invention to provide apparatus comprising the improved selective timing means.

It is another object of the present invention to provide improved gate control apparatus.

It is another object of the present invention to provide improved frequency measuring apparatus.

The present invention provides selective timing means comprising logic means to divide the frequency of a pulsed input signal by a number B, a reset input for setting said logic means to an initial state in response to a signal being applied thereto, a drive input for altering said initial state by one input in response to each signal pulse being applied thereto, a first output for producing signals representing a number stored in said logic means, a second output for producing a true level signal in response to the logic means being in a first cycle of operation, a third output for producing a true level signal in response to said logic means being in said initial state and a carry output for producing a signal in response to a number C being stored in said logic means, wherein C is an integer greater than unity and said first cycle of operation

begins upon a signal being applied to the reset input and ends when a number B of signal pulses have been applied to the drive input of said logic means; decoder means having an input connected to said first input and having an output for producing a true level signal in response to a signal representing a number A appearing at said input, wherein $0 < A \leq B-1$; first gating means having an input connected to the output of said decoder means, an input connected to said second output and having an output for producing a true level signal in response to a number A being stored in said logic means during the first cycle of operation of said logic means; and second gating means having an input connected to the output of said first gating means, an input connected to said third output, and having an output for producing a true level signal in response to either the logic means being in an initial state or a number A being stored in said logic means during said first cycle of operation.

The present invention also provides apparatus comprising selective timing means as set forth in the last preceding paragraph and a third gating means having an input connected to the output of said second gating means, an input connected to said drive input and having a gated output for production of an output signal pulse in response to $A+1$ and $nB+1$ signal pulses appearing at said drive input wherein $n \geq 0$.

The present invention also provides apparatus comprising timing means as set forth in the last preceding paragraph but one, and a third gating means having a first input connected to the output of said second gating means, a second input, and a gated output for producing a signal at said output in response to true level signals at said first and second inputs.

The present invention also provides gate control apparatus comprising a plurality of apparatuses as set forth in the last preceding paragraph each of which provides a single stage of said gate control apparatus; means connecting together the reset inputs of each stage to simultaneously set each stage to an initial state upon a signal being applied at any reset input; means connecting the drive input of a first stage to the second input of the third gating means of that first stage; means connecting the carry output of a preceding stage to the drive input of a succeeding stage; means connecting the gated output of the third gating means of a preceding stage to the second input of the third gating means of a succeeding stage for producing a signal at the gated output of a last stage of said gate control apparatus in response to AB^0+1 , $AB^1+1 \dots AB^{x-1}+1$ and nB^x+1 signal pulses applied at the signal input of the first stage of said gate control apparatus, where x is an integer representing the number of

stages in said gate control apparatus and $n \geq 0$.

The present invention also provides frequency measuring apparatus comprising a source of reference frequency signal pulses, gate control apparatus as set forth in the last preceding paragraph, decade counting and display means having an input and having an output responsive to the number of pulses of the signal which have been applied to said input for displaying said number in digitized form; switching means having an output connected to the input of said decade counting and display means and having a first input connected to receive an input signal to be counted, a second input and a third connected to the gated output of the last stage of said gate control apparatus for connecting the input signal to be counted at said first input to the output of said switching means in response to a signal appearing at said third input of said switching means and for disconnecting said input signal to be counted from the output of said switching means in response to the first signal that appears at said third input after a signal has appeared at said second input; means having an input connected to the output of said decade counting and display means and having an output connected to the second input of said switching means for applying a signal thereto in response to a certain number being registered in said decade counting and display means; and decimal point positioning means having an input connected to the gated output of the third gating means of said last stages and producing an output, in response to the number of signal pulses appearing at said gated input, for displaying a decimal point.

Preferably in frequency measuring apparatus as set forth in the last preceding paragraph said means having an output connected to said second input is also connected to the carry output from a stage of said gate control apparatus for applying a signal to said second input in response to a signal from said output of the decade counting and display means or from said carry output of said gate control apparatus.

There now follows a detailed description which is to be read with reference to the accompanying drawings of selective timing means, apparatus comprising the selective timing means, gate control apparatus and frequency measuring apparatus which are illustrative of the present invention; the selective timing means and the several apparatuses have been selected for description to illustrate the invention by way of example and not by way of limitation.

In the accompanying drawings:—

Figure 1 is a schematic representation of a single stage of a gate control apparatus according to the present invention;

Figure 2a to 2h show typical waveforms

produced by the apparatus shown in Figure 1;

Figure 3 is a block diagram of a gate control apparatus according to the present invention;

5 Figure 4 shows typical waveforms of a gate control apparatus according to the present invention; and

10 Figure 5 is a simplified block diagram of an automatic frequency measuring apparatus according to the present invention.

Referring now to Figure 1 there is shown apparatus providing a single stage of a gate control apparatus of the present invention. This single stage comprise selective timing means 11 according to the invention and the selective timing means 11 comprises logic means and first and second gating means 25 and 29 respectively. The logic means includes a counter 13 which is a conventional single digit counting assembly that may be, but is not limited to, a binary or a decimal counter, a recirculating shift register or other counting device. A reset signal applied to an input R of the selective timing means 11 causes the counter 13 to reset to an initial state. The initial state is determined by the particular design of the counter 13 and for the purpose of this description the initial state will be that state which causes the counter 13 to register the number zero (0). A train of periodic pulses as shown in Figure 2a is applied to the counter 13 through a drive input I of the selective timing means 11. The first input pulse following a reset signal causes the counter to advance from zero to one and each input pulse thereafter advances the counter 13 by one count. When the counter 13 has advanced B counts, where B is an integer determined by the design of the counter, the counter resets to its initial state. B will be assumed to be four (4) for the purpose of this description.

The counter 13 has a first output 15 connected to a conventional decoder 16 for producing a first signal representing the number of counts registered in the counter. The decoder 16 produces a true level at an output 17 in response to a signal representing A counts appearing at the output 15 of the counter 13 and produces a false level at the output 17 in response to a signal at the output 15 of the counter 13 representing other counts. The value of A is determined by the design of the decoder and this may be one or more integers such that $1 \leq A \leq (B-1)$. Therefore, with $B=4$, $A=1, 2$ or 3.

A second output 18 of the counter 13 is connected to a first logic element 14 of the logic means to produce a signal that indicates that the counter is in its first cycle of operation, i.e. between the time the counter has been reset by a reset signal applied at the input R of the selective timing means 11 and the time the counter advances B counts. The logic element 14 produces a true level at an

output 20 which provides a second output of the logic means, in response to its detecting the first cycle of operation of the counter 13 and produces a false level at the output 20 in response to the counter being in subsequent cycles.

The outputs 17 and 20 of the decoder 16 and the logic element 14, respectively, are connected to the input of first gating means provided by an AND gate 25. Figures 2a to 2e are graphs of typical waveforms produced by the apparatus in Figure 1 having the parameters $B=4$ and $A=2$. Figure 2c shows the output 27 of the AND gate 25 going to a true level 71 in response to the decoder 16 detecting A counts, i.e. two counts being registered in the counter 13 during the first cycle of operation of the counter.

The counter 13 has an output 21 connected to a second logic element 22 of the logic means for producing a signal whenever the counter 13 is in its initial state. The logic element 22 produces a true level at its output 23 which provides a third output of the logic means, in response to the counter 13 being in its initial state and produces a false level in response to the counter being in any other state. Figure 2b shows the output 23 of the logic element 22 going to a true level 81 in response to a reset signal being applied at the input R at time t_r and in response to the counter 13 resetting to its initial state after counting B counts, i.e. four counts.

The output 27 of the AND gate 25 and the output 23 of the logic element 22 are connected to the input of second gating means provided by an OR gate 29. The output of the OR gate 29 forms an output V of the selective timing means 11 and Figure 2d shows this output V going to a true level in response to a true level at either of its inputs.

Third gating means 41 in Figure 1 has two inputs I' and V' and an output T. The input V' is connected to the output V of the selective timing means 11 for enabling a gate 43 of the third gating means in response to a true level at output V.

Therefore, if the drive input I of the selective timing means 11 is connected to the signal pulse input I' of the gating means 41 and a train of pulses having a period of repetition T (as shown in Figure 2a) is applied to these inputs, pulse A+1 (pulse 3, $A=2$) and each pulse $nB+1$ (pulses 1, 5, 9 . . . $nB+1$, $B=4$) will be passed by the gate 43 to gating means output T. These pulses will occur at times $t=t_2, t_6, t_{10}, t_{14}, \dots, t_{4n}$, respectively, as shown in Figure 2e.

The counter 13 has an additional output which forms an output U of the selective timing means 11. Each time the number B is registered in the counter a signal (herein called a carry signal) appears at this output. To determine when a first carry signal will occur following a reset signal it is necessary

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to known the initial state of the counter. If, for example, $B=4$ and the initial state of the counter is that state which causes the counter to register the number one (1), the first carry signal will occur in response to the third signal pulse applied to the counter. Thereafter, carry signals will occur in response to every subsequent B signal pulse applied to the counter. Therefore, a carry signal occurs in response to $C+nB$ signal pulses appearing at drive input I of selective timing means 11 following a reset signal, where C is an integer defined by $(A+1) \leq C \leq B$. Figure 2f shows carry signals produced by the apparatus in Figure 1 for $B=4$, $A=2$ and $C=3$. A carry signal 107 occurs after C pulses, a carry signal 109 occurs after $C+1B$ ($3+4$) pulses and a carry signal 111 occurs after $C+2B$ pulses, etc.

To aid the reader in understanding the relationship between the parameters A and B, the output V of the selective timing means 11 is shown in Figure 2g for $B=4$, $A=1$. A first pulse into the counter 13 after a reset signal has appeared at the input R causes the counter to advance from its initial state and to register one count. Thereby the output 23 of the logic element 22 switches to a false level causing the output V of the selective timing means 11 to momentarily switch to a false level. Concurrently, the decoder 16 and the logic element 19 have detected A (one) counts being registered by the counter 13 during the first cycle of operation and the output 27 of the AND gate 25 switches to a true level causing the output V of the selective timing means 11 to return to a true level. This is indicated in Figure 2g as a pulse 115. Assuming that the inputs I and I' are connected together and a pulse train as shown in Figure 2a is applied to these inputs, pulses will be gated through the gating means 41 to the output T as shown in Figure 2h.

Thus, for a single stage of gate control apparatus according to the invention having both the drive and the signal pulse inputs connected to a source of signal pulses having a period of repetition T, the output signals will appear at the gated output at times $t=AT$, and $t=nBT=0, BT, 2BT, \dots, nBT$.

Referring now to Figure 3 there is shown a block representation of a gate control apparatus according to the present invention, the apparatus comprising a number of stages, each similar to the stage shown in Figure 1. The first stage 311 has inputs I_1 and I'_1 connected together. All stages have a common reset line. The carry output U of preceding stages is connected to the drive input I of succeeding stages and the gated output T of preceding stages is connected to the signal pulse input I' of succeeding stages.

It can be shown that if all stages of the gate control apparatus have identical parameters A, B and C, and an input signal having a

period of repetition T is applied to the input I_1 and I'_1 of the first stage, an output pulse will appear at the output T_x (the gated output of the xth stage) at times $t=AB^0T$, $t=AB^1T \dots AB^{x-1}T$ and $t=nB^xT$. In like manner it can be shown that for each input signal pulse AB^0+1 , $AB^1+1 \dots AB^{x-1}+1$ and nB^x+1 at inputs I_1 and I'_1 , and output signal will appear at the output T_x .

Figures 4a to 4i represent typical waveforms of a three stage ($x=3$) gate control apparatus according to the invention, each stage having parameters $A=2$, $B=4$, $C=4$. A train of periodic clock signals (Figure 4a) is applied to the input of the first stage of the gate control apparatus. The output of the selective timing means for the first stage appears in Figure 4b. Following a reset signal being applied at the reset input of the gate control apparatus, an output signal appears (Figure 4c) at the output T_1 of the first stage in response to AB^0+1 and nB^x+1 input signals. A carry signal appears (Figure 4d) at the output U_1 of the first stage in response to $C+nB$ input signals.

The carry output of the first stage provides signals to the drive input of the second stage. The output of the selective timing means of the second stage appears in Figure 4e. Output signals appear (Figure 4f) at the output T_2 of the second stage in response to AB^0+1 , AB^1+1 and nB^x+1 input signals at the drive input I_1 of the first stage. A carry signal appears (Figure 4g) at the output U_2 of the second stage in response to $C+nB$ signals into the drive input of that stage.

The carry output of the second stage provides signals to the drive input of the third stage. The output of the selective timing means of the third stage appears in Figure 4h. Output signals appear (Figure 4i) at the output T_3 of the third stage in response to AB^0+1 , AB^1+1 , AB^2+1 and nB^x+1 input signals at the drive input I_1 of the first stage.

Figures 4a to 4c and 4j to 4n represent typical waveforms for a three stage ($x=3$) gate control apparatus, each stage having parameters $A=2$, $B=4$, and $C=3$. These figures demonstrate the effect of making $C < B$.

Referring now to Figure 5 there is shown a simplified block diagram of an automatic frequency measuring apparatus according to the present invention. Gate control apparatus 511 forms the heart of the present invention. The apparatus 511 is shown having six stages ($x=6$) and for this example $A=1$, $B=10$, $C=10$.

A conventional decade counting and display assembly 513 counts and displays up to six digits of information and it has an input 543 for receiving an unknown input signal to be counted, a reset input to reset the assembly 513 to an initial state and an output 541 for providing a signal whenever a nine (9) is registered in the fifth decade. The

output 541 is connected to an input of an OR gate 517.

A reference frequency source 527 having an output 533 is connected to an input 535 of a pulse shaper 529. The pulse shaper output 537 is then connected to a drive input A of the gate control apparatus 511.

A signal having an unknown frequency is connected to an input B of an AND gate 519 of switching means of the frequency measuring apparatus. The AND gate 519 has its output connected to the input 543 of the decade counting and display assembly 513.

A reset signal is applied to the frequency measuring device at the reset inputs shown in Figure 5. The decade counting and display assembly 513 is set to an initial state of 000000. A D-type flip-flop 525 of the switching means is reset causing an output Q to be at a false level and thereby disabling the

AND gate 519. An output $\bar{Q}$ of a flip-flop 515 of the switching means goes to a true level in response to the reset signal and arms the "D" input of the flip-flop 525.

A first signal pulse appearing at the drive input A of the gate control apparatus 511 following the reset signal will be gated through the apparatus 511 and will appear at the gated output T_c of the last stage. The output T_c is connected to a decimal-point-positioning-and-units register 523 and to the clock input of the flip-flop 525. This first signal pulse causes the flip-flop 525 to set the output Q to a true level, enabling the AND gate 519 and thereby permitting the unknown input frequency to be passed to the decade counting and display assembly 513. Subsequent signal pulses from the output T_c of the gate control apparatus 511 will not cause the flip-flop 525 to reset until the flip-flop 515 is set again and therefore they will not terminate the time interval during which the unknown frequency is being counted. These subsequent signal pulses occur at times $t=1T$ i.e. $=(AB^0T)$, $10T$ i.e. $=(AB^1T)$, $100T$, 10^2T , 10^4T , 10^5T and $t=n10^6T$ i.e. $=(nB^6T)$. If the period of repetition of the reference frequency source is chosen to be $T=10^{-6}$ sec., the time intervals which are generated will be $1\mu s$, $10\mu s$, $100\mu s$, $1ms$, $10ms$, $100ms$, $1sec$, $2sec$, $2sec$, etc.

The first signal pulse from the output T_c of the gate control apparatus 511 that appears after the flip-flop 515 has been set will cause the flip-flop 525 to change states, disable the AND gate 519 and thereby terminate the time interval during which the unknown input signal was counted. While $n<2$, each time interval generated by the gate control apparatus 511 increases the time interval by a factor of ten. The flip-flop 515 should be set therefore when the decade counting and display assembly 513 reaches a value of approximately 10% of full scale. This will cause the

time interval to be terminated prior to the assembly 513 overflowing. When a nine (9) is detected in the fifth decade of the assembly 513 (i.e. 9% full scale), a signal will appear at the output 541 to set the flip-flop 515.

To obtain the best measurement possible within the time range of the gate control apparatus the carry output U_c from the last stage of the gate control apparatus 511 is also connected to the OR gate 517. This will cause the time interval to terminate at some time before $n=2$, and therefore each time interval generated will be ten times longer than the preceding one. The register 523 counts the number of pulses coming from the output T_c and shifts a decimal point in response to the count. The units (Hz, kHz, etc.) are also determined by the count.

Alternatively, the output 541 of the assembly 513 could be connected to set the flip-flop 515 in response to other numbers being registered in one or more of the decades and the carry output of any stage in the gate control apparatus 511 could be used to set the flip-flop 515.

It can be shown that if the frequency reference source 527 is connected to the input B of the AND gate 519 and an unknown signal having a period T is connected to the input 535 of the pulse shaper 537, upon the initiation of a measurement the average period of a number of periods of the unknown signal will be measured and the number of periods averaged will be determined automatically after the initiation of the measurement.

Therefore, the frequency measuring device can automatically determine the time interval during which the frequency of an unknown input signal is to be counted after the initiation of a measurement so that the greatest accuracy can be achieved in a single measurement. The device can also be used to automatically determine the number of periods of an unknown input signal that are to be averaged.

WHAT WE CLAIM IS:—

1. Selective timing means comprising logic means to divide the frequency of a pulsed input signal by a number B, a reset input for setting said logic means to an initial state in response to a signal being applied thereto, a drive input for altering said initial state by one count in response to each signal pulse being applied thereto, a first output for producing signals representing a number stored in said logic means, a second output for producing a true level signal in response to the logic means being in a first cycle of operation, a third output for producing a true level signal in response to said logic means being in said initial state and a carry output for producing a signal in response to a number C being stored in said logic means, wherein C is an integer greater than unity and said first



output 541 is connected to an input of an OR gate 517.

A reference frequency source 527 having an output 533 is connected to an input 535 of a pulse shaper 529. The pulse shaper output 537 is then connected to a drive input A of the gate control apparatus 511.

A signal having an unknown frequency is connected to an input B of an AND gate 519 of switching means of the frequency measuring apparatus. The AND gate 519 has its output connected to the input 543 of the decade counting and display assembly 513.

A reset signal is applied to the frequency measuring device at the reset inputs shown in Figure 5. The decade counting and display assembly 513 is set to an initial state of 000000. A D-type flip-flop 525 of the switching means is reset causing an output Q to be at a false level and thereby disabling the

AND gate 519. An output $\bar{Q}$ of a flip-flop 515 of the switching means goes to a true level in response to the reset signal and arms the "D" input of the flip-flop 525.

A first signal pulse appearing at the drive input A of the gate control apparatus 511 following the reset signal will be gated through the apparatus 511 and will appear at the gated output T_n of the last stage. The output T_n is connected to a decimal-point-positioning-and-units register 523 and to the clock input of the flip-flop 525. This first signal pulse causes the flip-flop 525 to set the output Q to a true level, enabling the AND gate 519 and thereby permitting the unknown input frequency to be passed to the decade counting and display assembly 513. Subsequent signal pulses from the output T_n of the gate control apparatus 511 will not cause the flip-flop 525 to reset until the flip-flop 515 is set again and therefore they will not terminate the time interval during which the unknown frequency is being counted. These subsequent signal pulses occur at times $t=1T$ i.e., (AB^0T) , $10T$ i.e., (AB^1T) , $100T$, 10^3T , 10^4T , 10^5T and $t=n10^nT$ i.e., (nB^nT) . If the period of repetition of the reference frequency source is chosen to be $T=10^{-6}$ sec., the time intervals which are generated will be $1\mu s$, $10\mu s$, $100\mu s$, $1ms$, $10ms$, $100ms$, 1 sec, 2 sec, etc.

The first signal pulse from the output T_n of the gate control apparatus 511 that appears after the flip-flop 515 has been set will cause the flip-flop 525 to change states, disable the AND gate 519 and thereby terminate the time interval during which the unknown input signal was counted. While $n < 2$, each time interval generated by the gate control apparatus 511 increases the time interval by a factor of ten. The flip-flop 515 should be set therefore when the decade counting and display assembly 513 reaches a value of approximately 10% of full scale. This will cause the

time interval to be terminated prior to the assembly 513 overflowing. When a nine (9) is detected in the fifth decade of the assembly 513 (i.e. 9% full scale), a signal will appear at the output 541 to set the flip-flop 515.

To obtain the best measurement possible within the time range of the gate control apparatus the carry output U_n from the last stage of the gate control apparatus 511 is also connected to the OR gate 517. This will cause the time interval to terminate at some time before $n=2$, and therefore each time interval generated will be ten times longer than the preceding one. The register 523 counts the number of pulses coming from the output T_n and shifts a decimal point in response to the count. The units (Hz, kHz, etc.) are also determined by the count.

Alternatively, the output 541 of the assembly 513 could be connected to set the flip-flop 515 in response to other numbers being registered in one or more of the decades and the carry output of any stage in the gate control apparatus 511 could be used to set the flip-flop 515.

It can be shown that if the frequency reference source 527 is connected to the input B of the AND gate 519 and an unknown signal having a period T is connected to the input 535 of the pulse shaper 537, upon the initiation of a measurement the average period of a number of periods of the unknown signal will be measured and the number of periods averaged will be determined automatically after the initiation of the measurement.

Therefore, the frequency measuring device can automatically determine the time interval during which the frequency of an unknown input signal is to be counted after the initiation of a measurement so that the greatest accuracy can be achieved in a single measurement. The device can also be used to automatically determine the number of periods of an unknown input signal that are to be averaged.

WHAT WE CLAIM IS:—

1. Selective timing means comprising logic means to divide the frequency of a pulsed input signal by a number B, a reset input for setting said logic means to an initial state in response to a signal being applied thereto, a drive input for altering said initial state by one count in response to each signal pulse being applied thereto, a first output for producing signals representing a number stored in said logic means, a second output for producing a true level signal in response to the logic means being in a first cycle of operation, a third output for producing a true level signal in response to said logic means being in said initial state and a carry output for producing a signal in response to a number C being stored in said logic means, wherein C is an integer greater than unity and said first



cycle of operation begins upon a signal being applied to the reset input and ends when a number B of signal pulses have been applied to the drive input of said logic means; decoder means having an input connected to said first output and having an output for producing a true level signal in response to a signal representing a number A appearing at said input, wherein $0 < A \leq B - 1$; first gating means having an input connected to the output of said decoder means, an input connected to said second output and having an output for producing a true level signal in response to a number A being stored in said logic means during the first cycle of operation of said logic means; and second gating means having an input connected to the output of said first gating means, an input connected to said third output, and having an output for producing a true level signal in response to either the logic means being in an initial state, or a number A being stored in said logic means during said first cycle of operation.

2. Apparatus comprising selective timing means according to Claim 1 and a third gating means having an input connected to the output of said second gating means, an input connected to said drive input and having a gated output for production of an output signal pulse in response to $A + 1$ and $nB + 1$ signal pulses appearing at said drive input wherein $n \geq 0$.

3. Apparatus comprising selective timing means according to Claim 1 and a third gating means having a first input connected to the output of said second gating means, a second input, and a gated output for producing a signal at said output in response to true level signals at said first and second inputs.

4. Gate control apparatus comprising; a plurality of apparatus according to Claim 3, each of which provides a single stage of said gate control apparatus; means connecting together the reset inputs of each stage to simultaneously set each stage to an initial state upon a signal being applied at any reset input; means connecting the drive input of a first stage to the second input of the third gating means of that first stage; means connecting the carry output of a preceding stage to the drive input of a succeeding stage; means connecting the gated output of the third gating means of a preceding stage to the second input of the third gating means of a succeeding stage for producing a signal at the gated output of a last stage of the gate control apparatus in response to $AB^0 + 1, AB^1 + 1, \dots, AB^{x-1} + 1$ and $nB^x + 1$ signal pulses applied at the signal input of the first stage of said gate control apparatus, where x is an integer

representing the number of stages in said gate control apparatus and $n \geq 0$.

5. Frequency measuring apparatus comprising; a source of reference frequency signal pulses; gate control apparatus according to Claim 4; decade counting and display means having an input and having an output responsive to the number of pulses of the signal which have been applied to said input for displaying said number in digitized form; switching means having an output connected to the input of said decade counting and display means and having a first input connected to receive an input signal to be counted, a second input, and a third input connected to the gated output of the last stage of said gate control apparatus for connecting the input signal to be counted at said first input to the output of said switching means in response to a signal appearing at said third input of said switching means and for disconnecting said input signal to be counted from the output of said switching means in response to the first signal that appears at said third input after a signal has appeared at said second input; means having an input connected to the output of said decade counting and display means and having an output connected to the second input of said switching means for applying a signal thereto in response to a certain number being registered in said decade counting and display means; and decimal-point-positioning means having an input connected to the gated output of the third gating means of said last stages and producing an output, in response to the number of signal pulses appearing at said gated output, for displaying a decimal point.

6. Apparatus according to claim 5, wherein said means having an output connected to said second input is also connected to the carry output from a stage of said gate control apparatus for applying a signal to said second input in response to a signal from said output of the decade counting and display means or from said carry output of said gate control apparatus.

7. Selective timing means according to Claim 1 substantially as hereinbefore described with reference to Figures 1 and 2 of the accompanying drawings.

8. Apparatus according to either one of Claims 2 and 3 substantially as hereinbefore described with reference to Figures 1 and 2 of the accompanying drawings.

9. Gate control apparatus according to Claim 4 substantially as hereinbefore described with reference to Figures 3 and 4 of the accompanying drawings.



10. Frequency measuring apparatus according to Claim 5 substantially as hereinbefore described with reference to Figure 5 of the accompanying drawings.

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