CLAIMS

1. An integrated circuit, comprising:

a pixel, comprising:

a photodetection region; and

a drain configured to discard charge carriers from within a semiconductor region of the pixel outside of the photodetection region.

2. The integrated circuit of claim 1, wherein the drain is configured such that the drain does not extract charge carriers from the photodetection region when the drain is biased at a voltage in an operational voltage range of the pixel.

3. The integrated circuit of claim 1 or claim 2, wherein the drain is maintained at a fixed voltage.

4. The integrated circuit of any one of claims 1-3, wherein a voltage of the drain is variable.

5. The integrated circuit of any one of claims 1-4, wherein the drain comprises a semiconductor region.

6. The integrated circuit of claim 5, further comprising a conductive contact that contacts the semiconductor region.

7. The integrated circuit of claim 6, wherein the conductive contact is a metal plug.

8. The integrated circuit of claim 6 or claim 7, wherein the conductive contact does not extend outside an area of the drain in plan view.

9. The integrated circuit of claim 5, wherein the semiconductor region is doped.

10. The integrated circuit of claim 9, wherein the semiconductor region is n-type doped.

11. The integrated circuit of claim 10, further comprising a second semiconductor region that is p-type doped under the semiconductor region that is n-type doped.

12. The integrated circuit of any one of claims 1-11, wherein the semiconductor region is spaced apart from the photodetection region.

13. The integrated circuit of any one of claims 1-12, wherein the drain is a first drain and the pixel further comprises a second drain.

14. The integrated circuit of claim 13, wherein the first drain is on a first side of the photodetection region and the second drain is on a second side of the photodetection region.

15. The integrated circuit of claim 13 or claim 14, wherein the pixel further comprises a third drain.

16. The integrated circuit of claim 15, wherein the third drain is within a readout region of the pixel.

17. The integrated circuit of claim 15 or claim 16, wherein the third drain is configured to discard carriers from the photodetection region.

18. The integrated circuit of any one of claims 1-17, wherein the drain comprises a pn junction or a Schottky junction.

19. The integrated circuit of any one of claims 1-18, wherein the drain establishes a depletion region that overlaps with a depletion region of the photodetection region.

20. The integrated circuit of any one of claims 1-19, wherein the drain is configured to collect and discard charge carriers under pixel circuitry or one or more doped regions.

21. The integrated circuit of any one of claims 1-20, wherein the drain is a first drain and the integrated circuit further comprises a second drain, wherein the second drain is configured to discard carriers from the photodetection region.

22. A method of manufacturing an integrated circuit, the method comprising:

forming a pixel comprising a photodetection region and a drain configured to discard charge carriers from within a semiconductor region of the pixel outside of the photodetection region.