

ABSTRACT

2-TRANSISTOR NONVOLATILE MEMORY CELL

A 2-transistor (2T) memory cell comprising a first transistor and a second transistor. The first and second transistors respectively have a source and a drain separated apart by a channel thereof, a floating gate over the channel near the source side, and a control gate over the floating gate and the channel near the drain side. The sources, floating gates, and control gates of the first and second transistors are respectively mutually connected. In addition, driving capability of the second transistor is substantially larger than that of the first transistor.

Figure 2A