

Claims

1. An electronic circuit configured and arranged for operating an event-driven spiking convolutional neural network (1), comprising a plurality of layers, wherein each layer comprises

- a kernel module (110) configured to store and to process in an event-driven fashion kernel values of at least one convolution kernel (410),

- a neuron module (120) configured to store and to update in an event-driven fashion neuron states of neurons of the spiking convolutional neural network (1), and to output spike events (150) generated from updated neurons (420),

- a destination mapper (170) configured to generate outgoing destination information of an outgoing spike event (150) received from the neuron module (120) of the current layer and to append said destination information to the outgoing spike event (150),

- a memory mapper (130) configured to determine neurons (420) to which an incoming spike event (140) from a source layer projects by means of a convolution with at least one convolution kernel (410),

and wherein neuron states of said determined neurons (420) are to be updated with applicable kernel values of at least one convolution kernel (410),

wherein the memory mapper (130) is configured to process incoming spike events in an event-driven fashion.

2. The electronic circuit according to claim 1, wherein the kernel module (110) comprises a kernel interface (111) connected to an associated kernel memory (112), wherein the associated kernel memory (112) is configured to store the kernel values of the at least one convolution kernel

in kernel addresses, wherein the kernel module (110) is electronically connected to the neuron module (120).

3. The electronic circuit according to claim 1 or 2, wherein the memory mapper (130) is electronically connected to the kernel module (110), wherein the memory mapper (130) is configured and arranged

a) to receive the incoming spike event (140) from a source layer of the spiking neural network (1), the incoming spike event (140) comprising information on a neuron coordinate (421) in the source layer,

and in response to the received spike event (140),

b) to determine neuron coordinates (422) and corresponding neuron addresses of the neurons (420) to which a convolution of the received spike event (140) with the at least one convolution kernel (110) projects,

c) to determine kernel addresses with corresponding kernel coordinates (411) of the kernel values applicable to the neuron states of the determined neuron addresses, wherein the neuron states of the determined neuron addresses are to be updated with the applicable kernel values,

d) to provide the determined neuron addresses to the kernel module.

4. The electronic circuit according to claim 3, wherein the kernel module (110) is configured and arranged to receive the determined kernel addresses and to provide the applicable kernel values stored at the determined kernel addresses, in conjunction with the determined neuron addresses, to the neuron module (120).

5. The electronic circuit according to claim 3, wherein the neuron module (120) is configured and arranged

a) to receive the determined neuron addresses (142n) and the applicable kernel values (142k),

b) to determine for each received neuron address (142n) an updated neuron state for the neuron (420) based on the applicable kernel value (142k),

c) to output an outgoing spike event (150) for updated neurons (420) reaching at least one predefined threshold value (502).

6. The electronic circuit according to claim 1, wherein the memory mapper (130) is configured to determine for each received spike event (140) at least one output feature map (430) consisting of neurons assigned to the output feature map (430), wherein the number of output feature maps (430) is equal to the number of convolution kernels (410) of the current layer (10).

7. The electronic circuit according to claim 1, wherein each layer (10, 10') further comprises a bias module (160) comprising an associated bias memory (162) and a bias interface (161) connected to the associated bias memory (162), wherein the associated bias memory (162) is configured to store bias values in bias addresses, wherein the bias module (160) is connected to the neuron module (120) and wherein the bias module (160) is configured to provide predefined time-intervals bias values to the neuron module (120), wherein the neuron module (120) is configured to update the neuron states of all neurons (431) in at least one output feature map (430) based on the received bias values.

8. The electronic circuit according to claim 7, wherein the neuron module (120) comprises a plurality of parallel-operating neuron sub-interfaces (121s) that are configured to process received neuron addresses (142n) and kernel values (142k), and the received bias values (142b) and to generate (501, 502) updated neuron states and spike events (150), wherein

each neuron sub-interface (121s) has an associated neuron memory (506) for reading the neuron state for the received neuron address and to write the updated neuron state to the received neuron address in the associated neuron memory (506), such that a parallel processing of neuron state is achieved by the neuron sub-interfaces and their associated neuron memories (506).

9. The electronic circuit according to claim 8, wherein the neuron module (120) comprises a router module (601) configured and adapted to receive determined neuron addresses (142n) and kernel values (142k), and bias values (142b) from the kernel module (110) and/or a bias module (160), and to transmit the received neuron addresses (142n) and the kernel values (142k), and the bias values (142b) to the plurality of parallel-operating neuron sub-interfaces (121s) that are configured to process the received neuron addresses (142n) and kernel value (142k), and the bias values (142b) in parallel, wherein the neuron module further comprises a merger module (602) configured and adapted to receive generated spike events (150) from the plurality of neuron sub-interfaces (121s) and funnel the spike events for serial processing in a bus having less channels than neuron sub-interfaces, wherein the bus has a single transmission channel only.

10. The electronic circuit according to claim 9, wherein the neuron module (120) is configured

- to receive a neuron address (142n) and a kernel value (142k), and a bias value (142b) from the kernel module (110) and/or the bias module (160) at the router module (601),
- to read (500) a neuron state of the received neuron address (142n) from the associated neuron memory (506) on one of the neuron sub-interfaces (121s),

- to update (501) the read neuron state with the received kernel value (142k) and/or with the received bias value (142b) on the neuron sub-interface (121s),
- to compare the updated neuron state with at least one threshold value (502) stored in and accessible from a threshold register on the neuron sub-interface (121s),
- upon reaching the at least one threshold value (502), to generate a spike event (503) that is provided to a destination mapper (170), and to reset the updated neuron state to a reset neuron state,
- to write (505) the updated neuron state to the received neuron address (142n) of the associated neuron memory (506).

11. The electronic circuit according to claim 3, wherein the memory mapper (130) is configured to execute the following sequence of operations in order to determine the kernel addresses of the applicable kernel values (142k) and neuron coordinates (421) with the corresponding neuron addresses (142n) to be updated when a spike event (140) is received by the memory mapper (130), the spike event (140) comprising or consisting of an information about a coordinate (x,y) of a neuron (421) having generated the spike event (140) in a source feature map (440), and a channel identifier (c), the coordinate (x,y) comprising an x-identifier and y-identifier:

- zero padding (x+p_x, y+p_y) the coordinate (x,y) of the spike event (140) with a predefined offset (p_x, p_y) provided by and stored in a register,
- from the coordinate (x,y), from the zero-padded coordinate (x+p_x, y+p_y), computing a neuron anchor coordinate (x₀, y₀) to which the spike event projects, and a corresponding kernel anchor coordinate (x₀^k, y₀^k) of the at least one kernel (f), wherein the kernel anchor coordinate (x₀^k, y₀^k) is indicative of a kernel coordinate (f, x₀^k, y₀^k) for each of the at least one kernel

(f), wherein the neuron anchor coordinate (x_0, y_0) is associated to an output feature map (430),

- starting from the neuron anchor coordinate and the kernel anchor coordinate, determining all neuron coordinates (f, x, y) that are to be updated and all kernel coordinates (c, f, x^k, y^k) of the applicable kernel values (142k) by processing information on an output feature map (430) size, a stride size and/or a kernel size that are provided by a register,
- determining from the determined all neuron coordinates (f, x, y) and the all kernel coordinates (c, f, x^k, y^k) of the applicable kernel values (142k) compressed neuron addresses and compressed kernel addresses,
- providing the determined compressed neuron addresses and compressed kernel addresses to the kernel module (110) and/or the neuron module (120).

12. The electronic circuit according to claim 8, wherein the associated neuron memory (506) is organized such that all neuron states are stored in consecutive neuron addresses, wherein the memory mapper (130) is configured to generate for all neuron coordinates (f, x, y) in the consecutive neuron addresses such as to generate compressed neuron addresses and wherein the memory mapper (130) is configured to provide the compressed neuron addresses to the neuron module (120).

13. The electronic circuit according to claim 1, wherein the event-driven spiking convolutional network (1) comprises a plurality of layers (10, 10', 10'') that are connected with a spike event router (200) that is configured to route an outgoing spike event received from a source layer to at least one destination layer, wherein the spike event router (200) accesses the

destination information associated to the outgoing spike event (150), wherein the destination layer (10'') can be the source layer (10').

14. The electronic circuit according to claims 1 to 14, wherein the layer refers to at least one electronic circuit that represents a layer in the spiking convolutional neural network, and

the event-driven spiking convolutional neural network operates not frame-based or clock-based.

15. The electronic circuit according to claims 1 to 14, wherein the memory mapper (130), the neuron module (120) and the kernel module (110) have a hard-wired correspondence in the electronic circuit.

16. The electronic circuit according to claims 1 to 14, wherein the memory mapper (130) is an asynchronous electronic circuit.

17. The electronic circuit according to claims 3, wherein the memory mapper (130) is wired to execute a predefined formula that is configured to determine the neuron addresses that are to be updated by the applicable kernel values.

18. The electronic circuit according to claim 17, wherein the memory mapper (130) can be provided with programmable register values specifying the formula for said determination.

19. The electronic circuit according to claim 16, wherein the memory mapper (130) is an asynchronous serial interface circuit having a predefined

bandwidth parallel interface such that at least one spike event can be processed at a time.

20. The electronic circuit according to claim 16, wherein the spiking convolutional neural network is configured to receive asynchronous spike events and to process each spike event upon reception.

21. The electronic circuit according to claim 20, wherein the kernel module (110) is an asynchronous module and destination mapper (170) is an asynchronous electronic circuit.

22. The electronic circuit according to claims 1 to 14, wherein the plurality of layers that are electronically connected and organized by means of a spike event router which can be programmable so as to allow for various spiking convolutional neural network configurations and routing options.

23. The electronic circuit according to claim 22, wherein the spiking convolutional neural network is configured to receive and process spike events from a dynamic vision sensor, wherein the dynamic vision sensor configured to generate event-driven spikes can serve as an input or a first source layer for the spike event router.

24. The electronic circuit according to claim 2, wherein the associated kernel memory (112) is a memory that is physically arranged on each layer.

25. The electronic circuit according to claim 8, wherein each associated neuron memory (506) is a memory storage that is physically arranged on

each layer or a memory that is allocated and connected to the layer but not comprised by the layer.

26. The electronic circuit according to claims 1 to 14, wherein the memory mapper (130) starts processing the incoming spike event (140) once the incoming spike event (140) is received by the memory mapper (130), and the memory mapper (130) is event-driven and comprises a processing pipeline with multiple buffer stages and electronic combinatorial logistic circuits to add, multiply and multiplex various bits of the spike event c , x , and y , wherein the incoming spike event (140) comprises information about a coordinate (x, y) and a channel identifier (c) .

27. The electronic circuit according to claim 11, wherein the neuron anchor coordinate (x_o, y_o) is given by a neuron located in the bottom right corner of an array in the respective output feature map (430) to which the event projects, and

a corresponding kernel anchor coordinate (x_o^k, y_o^k) is calculated that corresponds to the neuron anchor coordinate (x_o, y_o) , and

the neuron anchor coordinate (x_o, y_o) and the kernel anchor coordinate (x_o^k, y_o^k) are then sent to an address sweep module (302) that is configured to compute the remaining neuron coordinates of the neurons (420) to which the incoming spike event (140) projects and their associated neuron addresses (142n).

28. The electronic circuit according to claims 1 to 14, wherein the registers of the layers are programmed in order to reflect the specific layout of each layer.

29. The electronic circuit according to claim 7, wherein the bias module (160) comprises a bias register (161) that stores an output feature map index indicative for the output feature maps in the current layer that are to be updated with the bias values.

30. The electronic circuit according to claims 1 to 14, wherein the destination mapper (170) is an event-driven and asynchronous electronic circuit.