FIG. 1

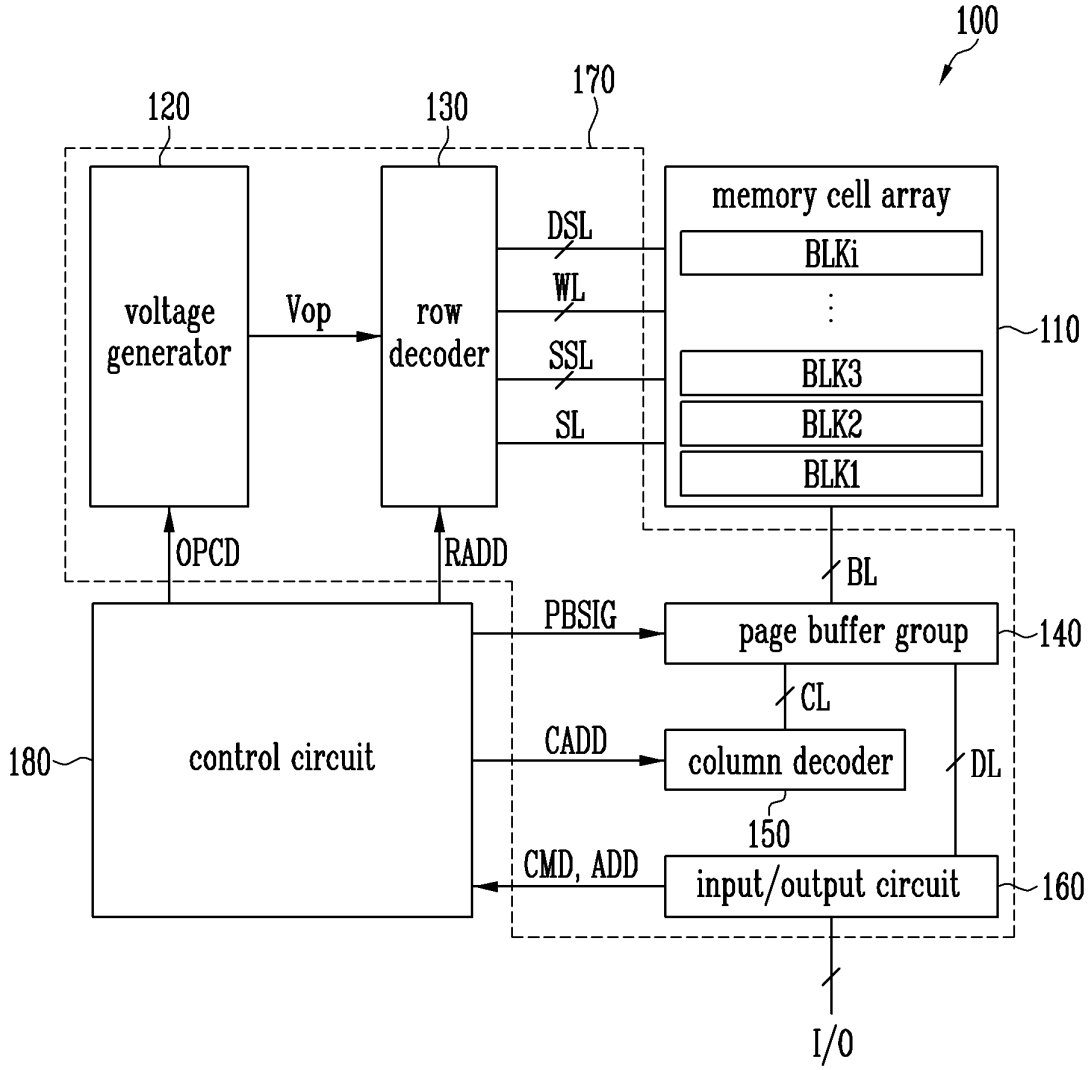

100
120
130
170
voltage generator
Vop
row decoder
DSL
WL
SSL
SL
memory cell array
BLKi
BLK3
BLK2
BLK1
110
OPCD
RADD
BL
PBSIG
page buffer group
140
CL
180
control circuit
CADD
column decoder
DL
150
CMD, ADD
input/output circuit
160
I/O

FIG. 2

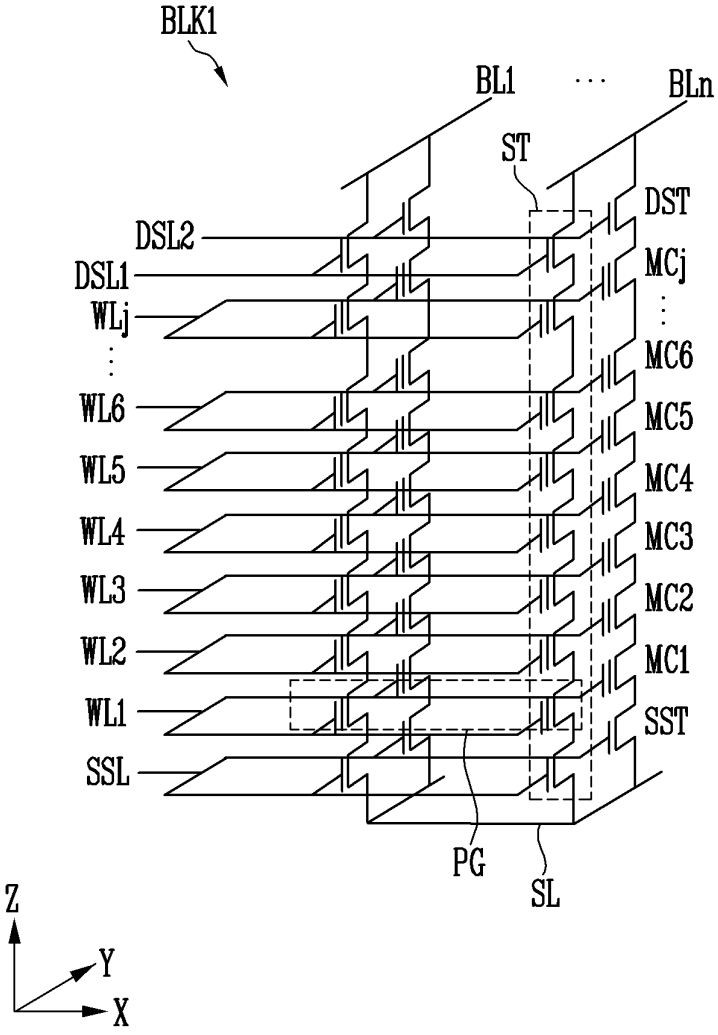

BLK1
BL1
BLn
ST
DST
DSL2
DSL1
WLj
MCj
MC6
WL6
MC5
WL5
MC4
WL4
MC3
WL3
MC2
WL2
MC1
WL1
SST
SSL
PG
SL
Z
Y
X

FIG. 3

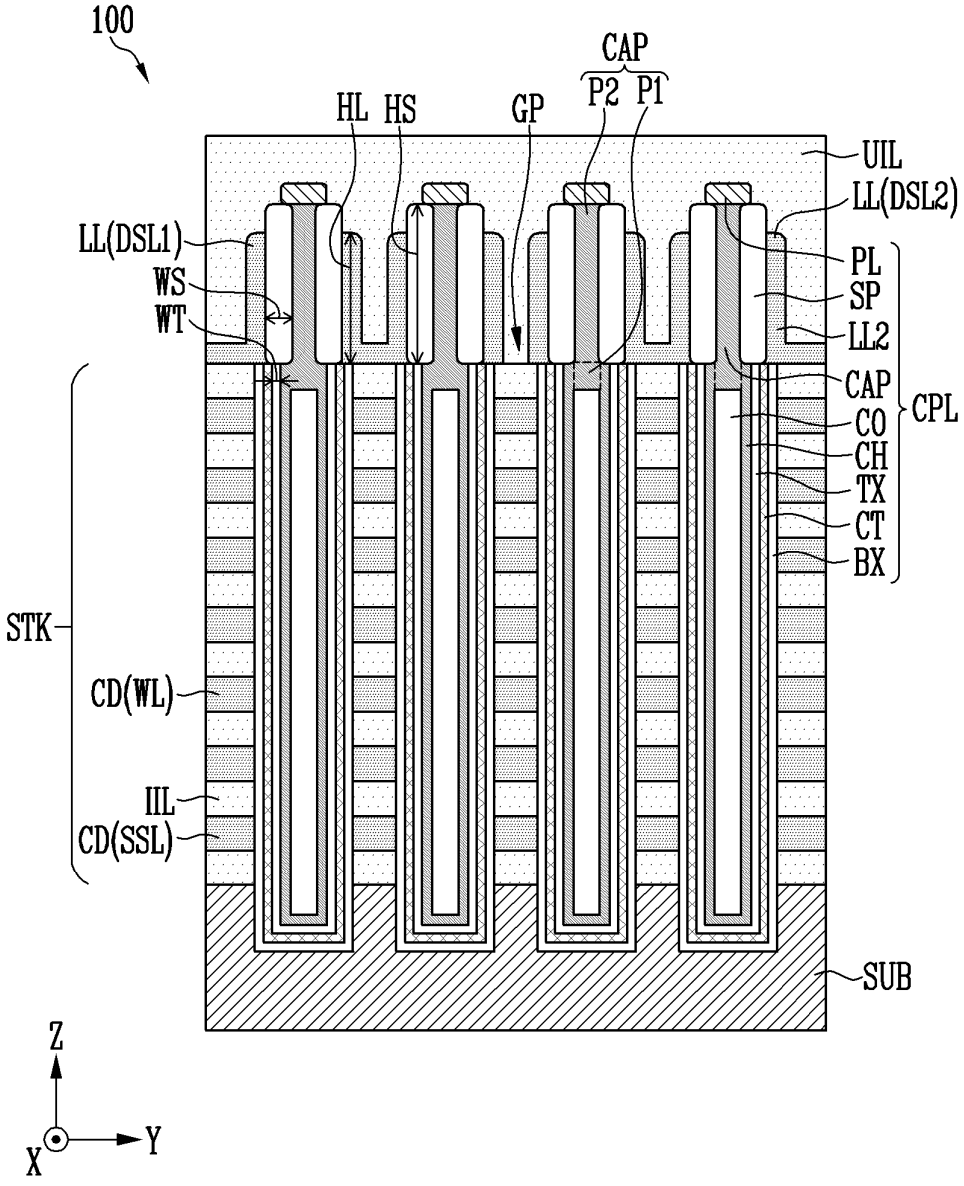

100
CAP
P2 P1
HL HS
GP
UIL
LL(DSL2)
LL(DSL1)
PL
WS
SP
WT
LL2
CAP
CPL
CO
CH
TX
CT
BX
STK
CD(WL)
IIL
CD(SSL)
SUB
Z
Y
X

FIG. 4A

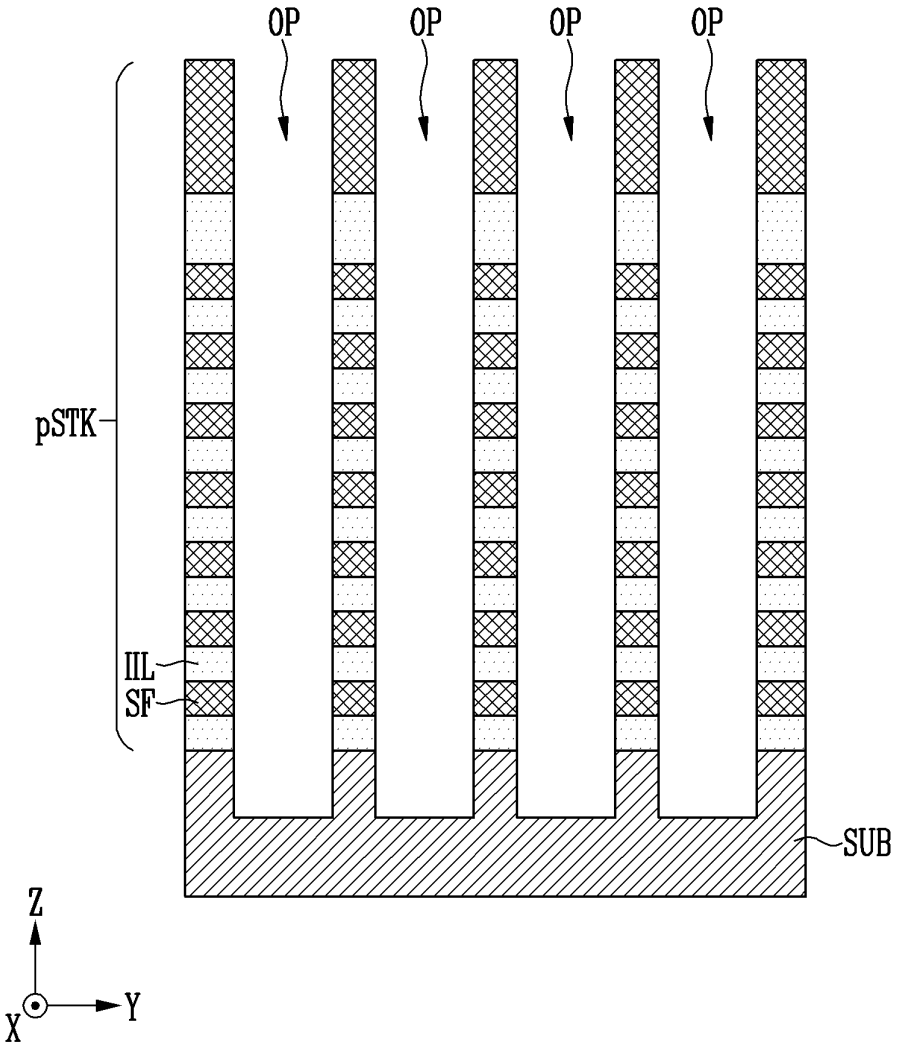


FIG. 4B

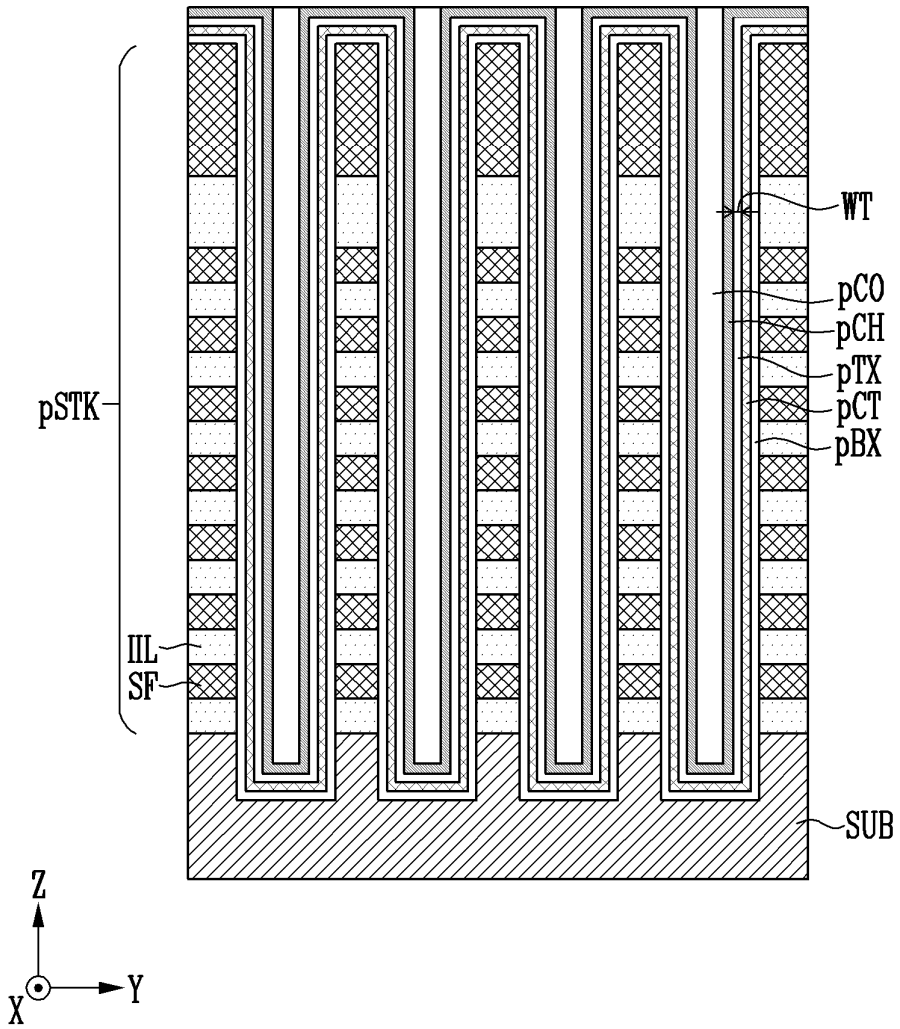


FIG. 4C

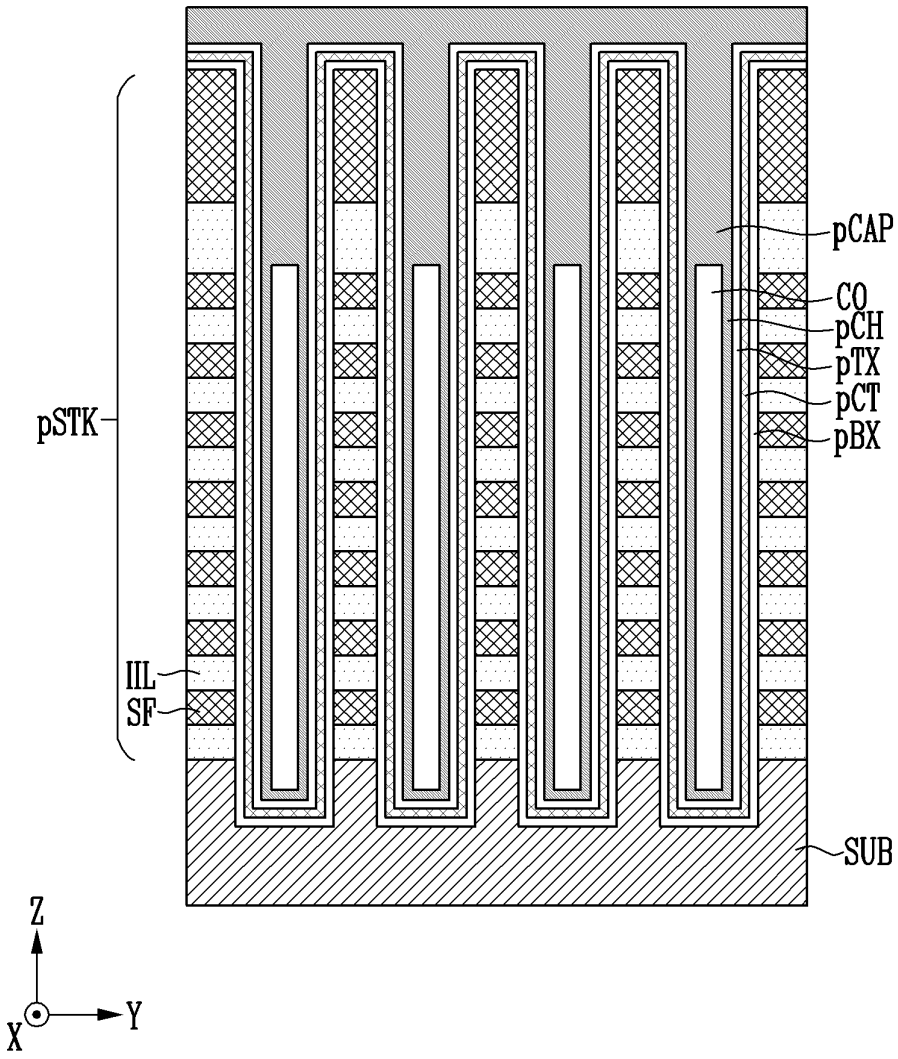


FIG. 4D

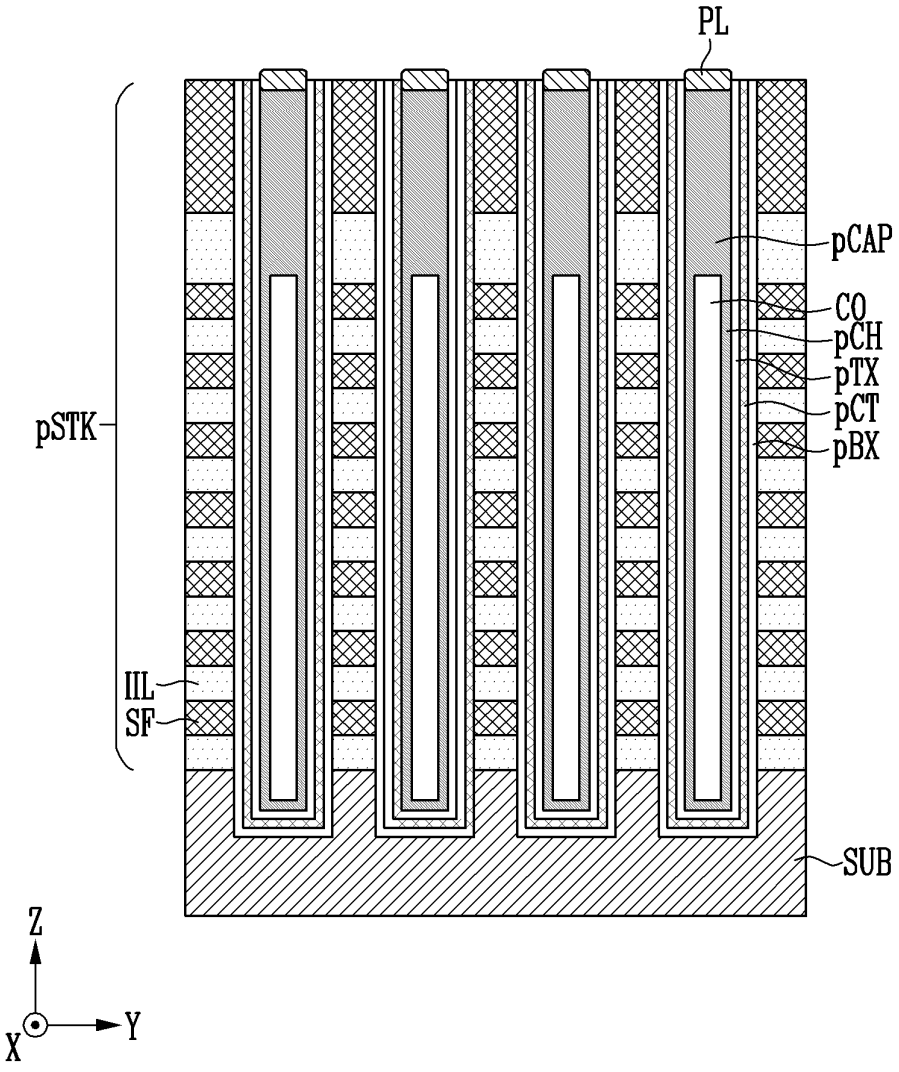


FIG. 4E

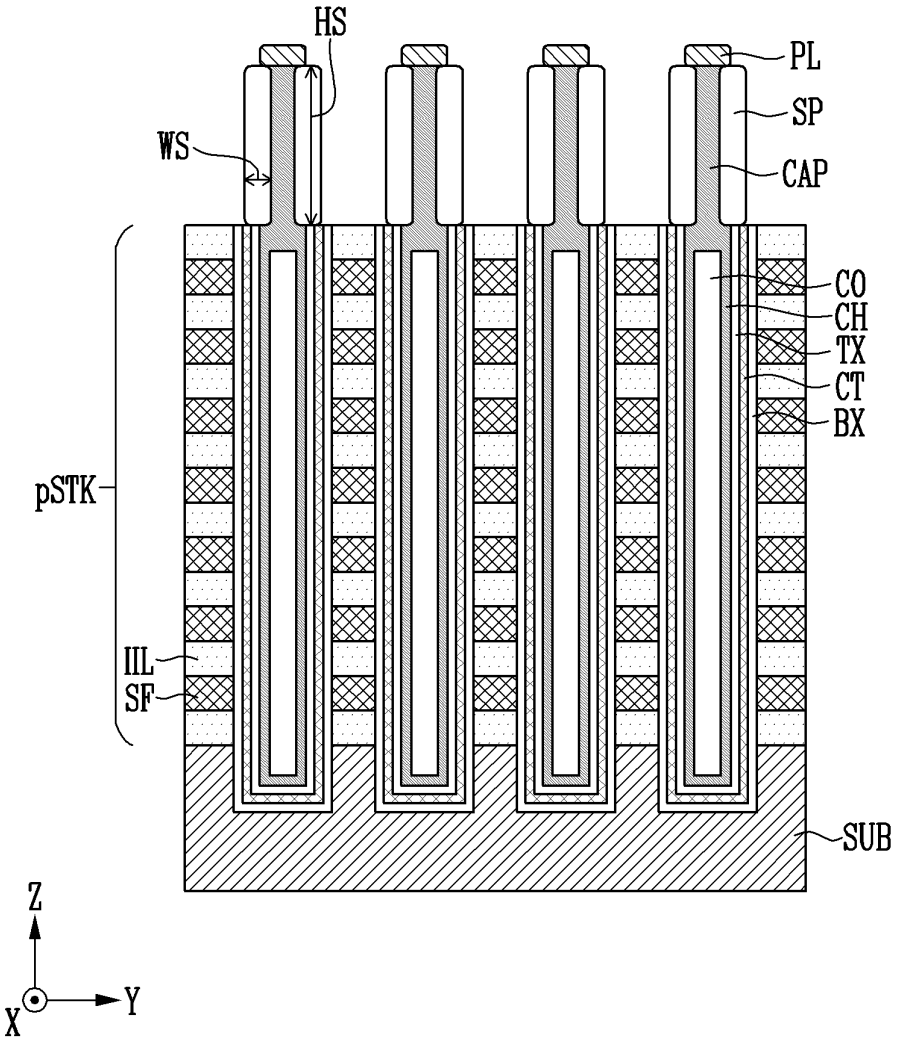


FIG. 4F

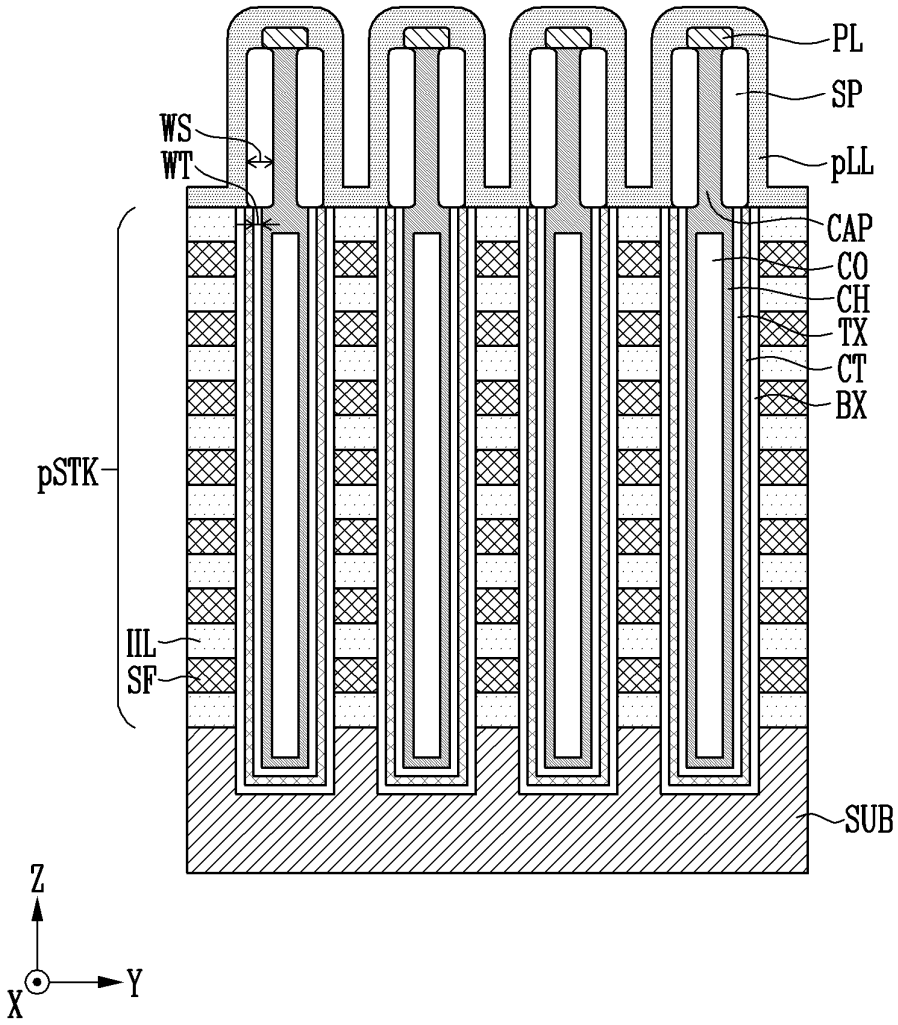


FIG. 4G

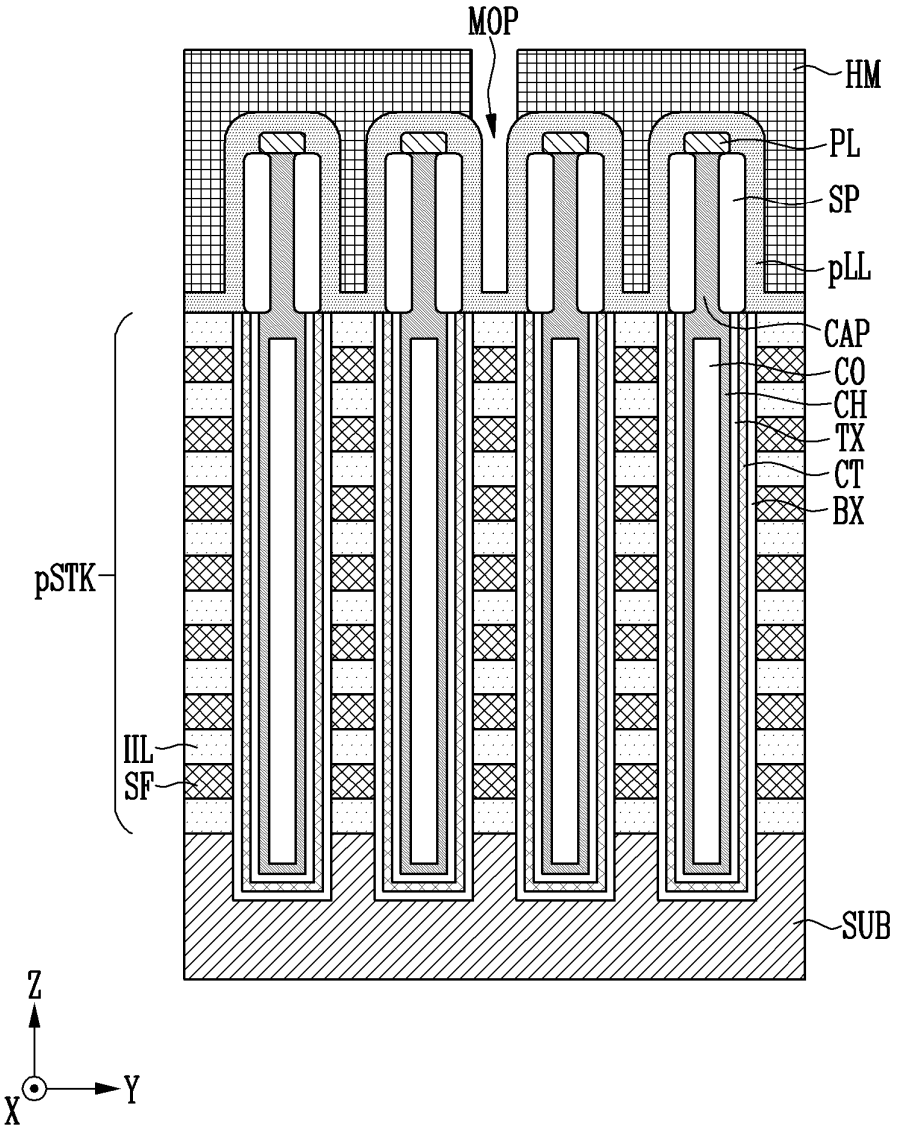


FIG. 4H

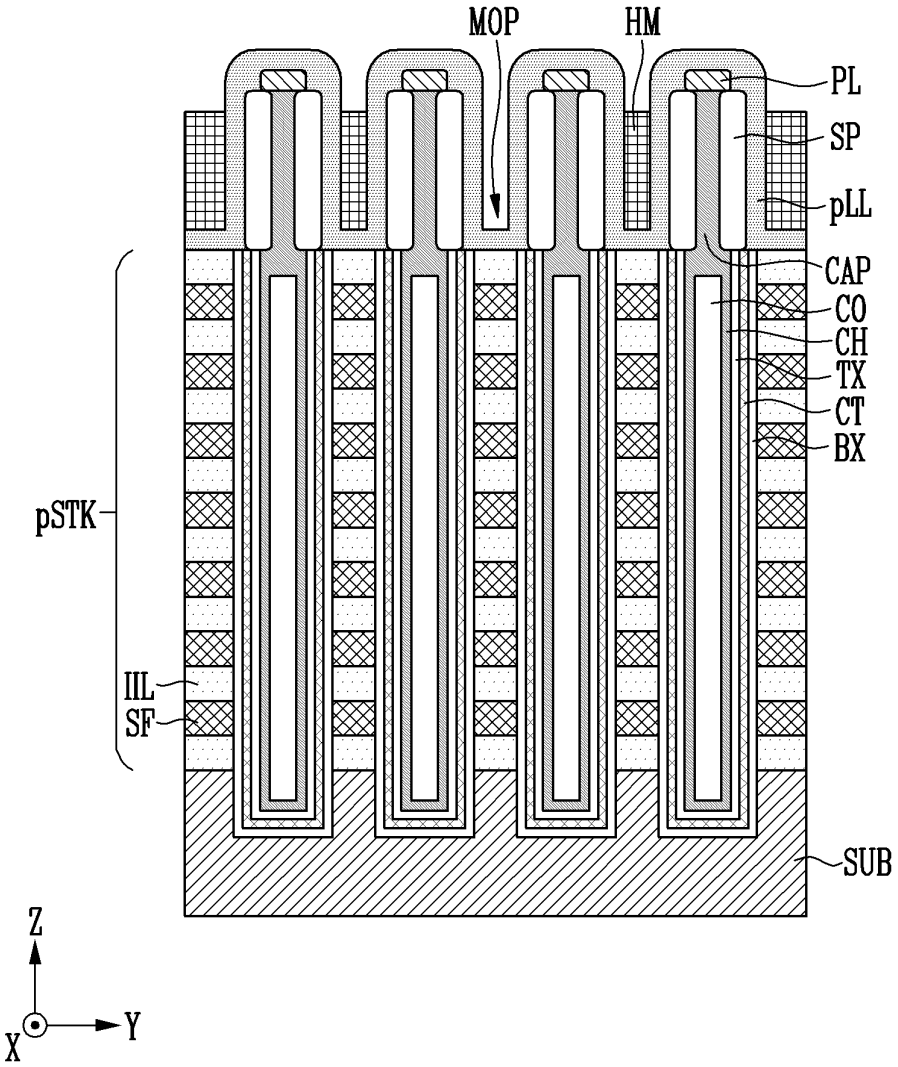


FIG. 4I

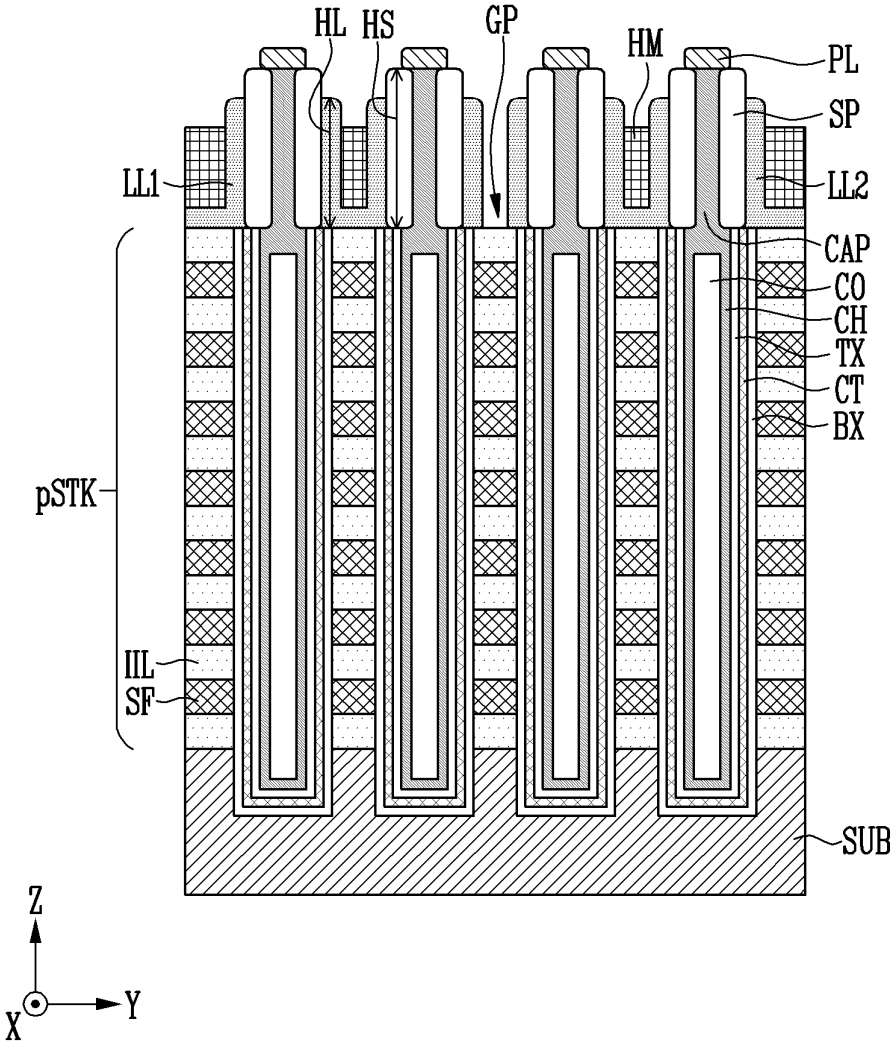


FIG. 4J

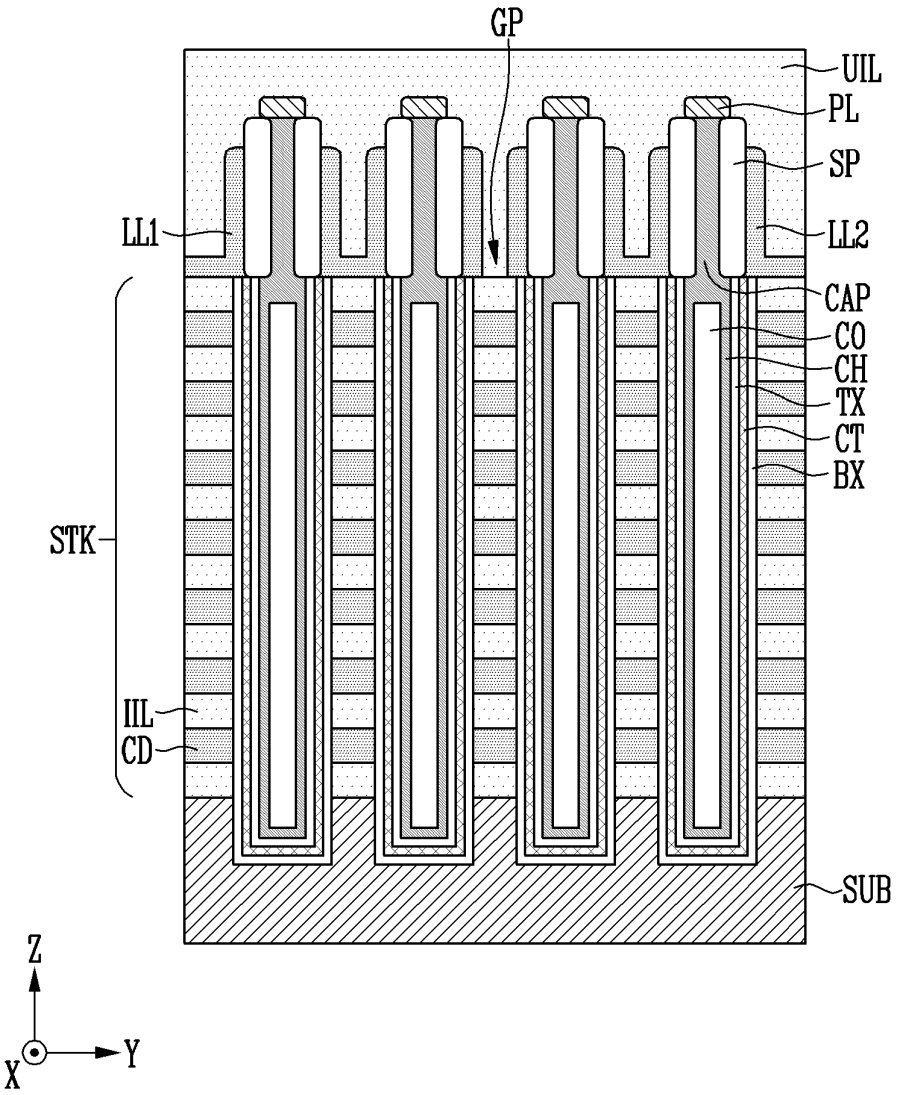


FIG. 5

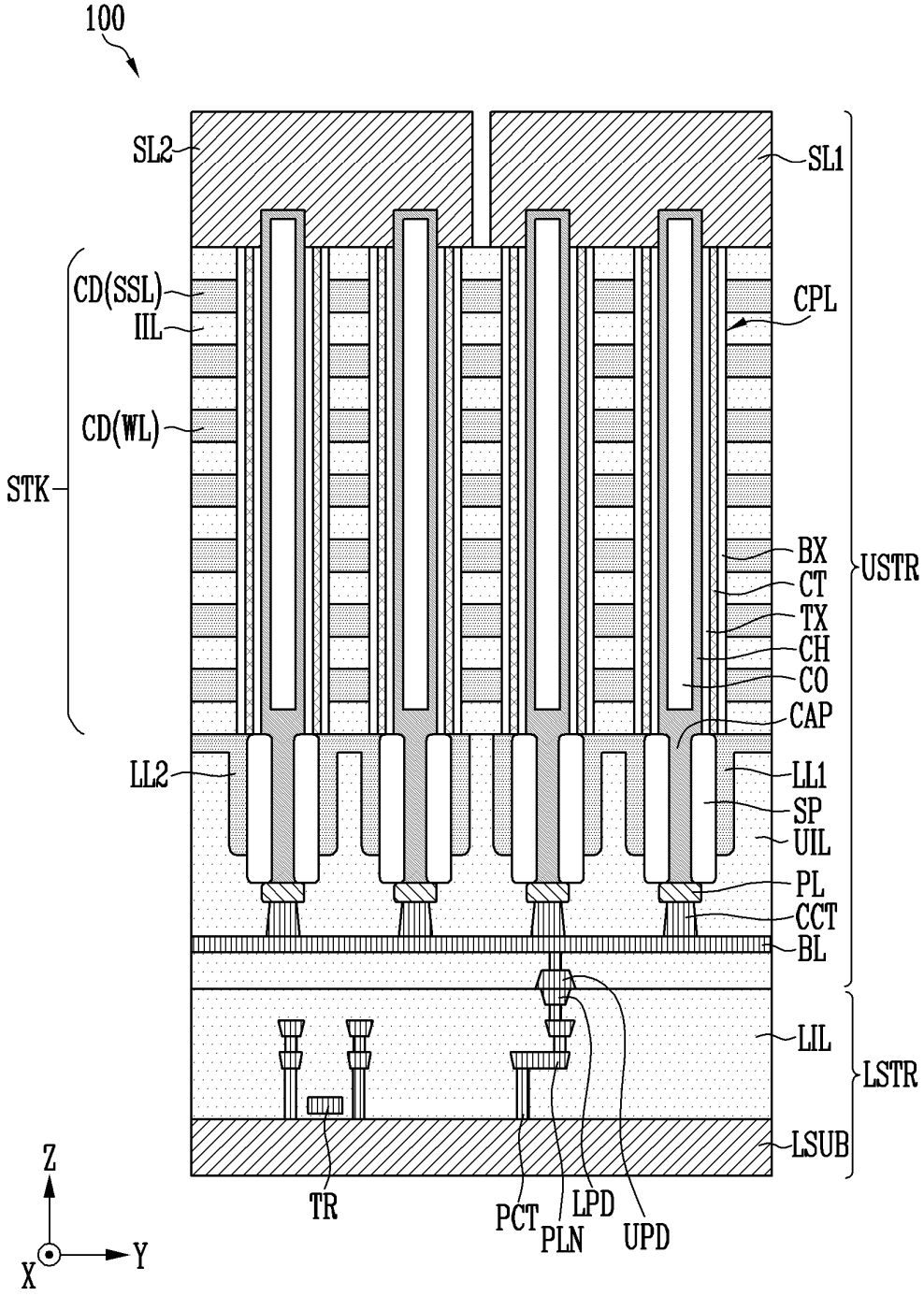

100
SL2
SL1
CD(SSL)
IIL
CPL
CD(WL)
STK
BX
CT
TX
CH
CO
CAP
USTR
LL2
LL1
SP
UIL
PL
CCT
BL
LIL
LSTR
LSUB
TR
PCT
PLN
LPD
UPD
Z
Y
X

FIG. 6

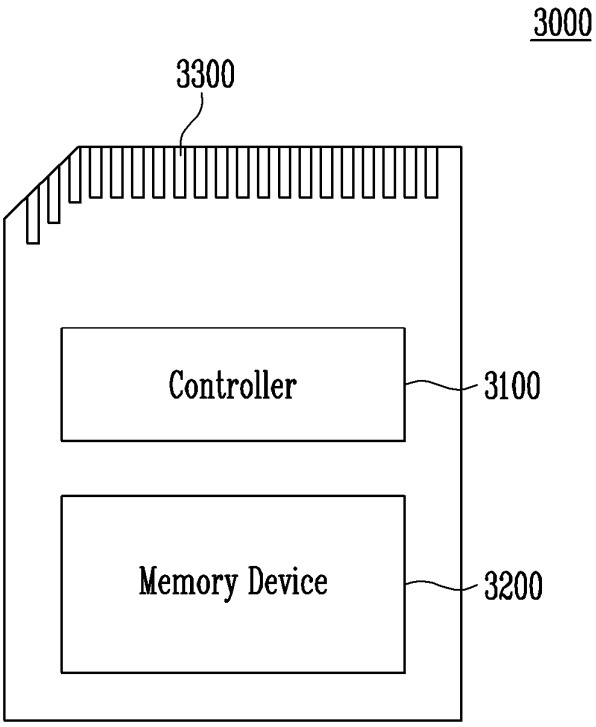
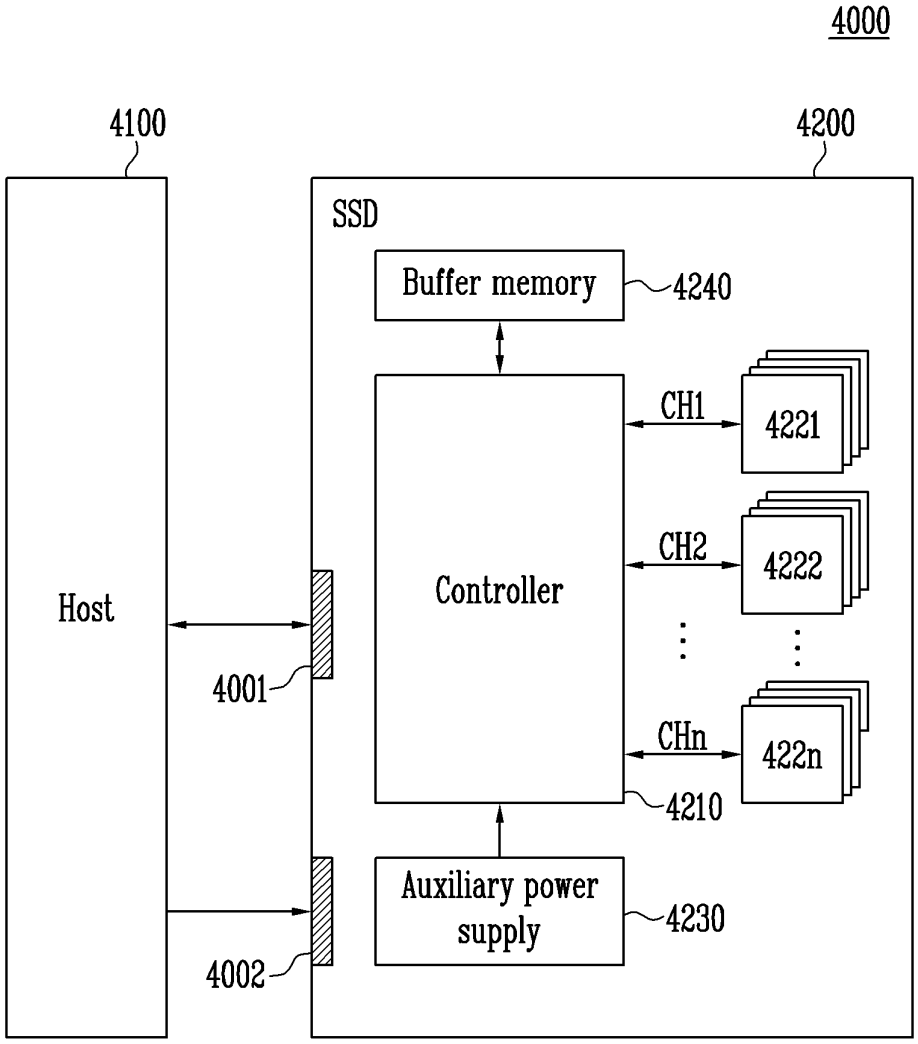


FIG. 7


4000
4100
4200
SSD
Buffer memory
4240
Host
Controller
CH1
4221
CH2
4222
CHn
422n
4210
4001
4002
Auxiliary power supply
4230