CLAIMS

1. A manufacturing method of a semiconductor structure, comprising:

providing a substrate, wherein the substrate comprises active regions and isolation regions, each of the isolation regions comprises a first trench and an isolation layer formed in the first trench, and a sacrificial layer is provided on the active regions;

removing the sacrificial layer and part of the isolation layer by an etching process to form first grooves, wherein a whole upper surface of the isolation layer is lower than upper surfaces of the active regions;

forming a first mask layer, wherein the first mask layer covers upper surfaces of the active regions and fills the first grooves;

planarizing the first mask layer, such that an upper surface of a portion of the first mask layer located above the active regions is flush with an upper surface of a portion of the first mask layer located above the isolation regions;

a first thickness of the portion of the first mask layer located above the isolation regions is greater than a second thickness of the portion of the first mask layer located above the active regions;

removing part of the first mask layer, part of the isolation layer, and part of the substrate, to form a second trench comprising second trench portions and third trench portions arranged alternatively in a direction, wherein a lower part of each of the second trench portions is located in a respective one of the isolation regions, a lower part of each of the third trench portions is located in a respective one of the active regions, and a width of each third trench portion is greater than a width of each second trench portion, and an upper part of each second trench portion in the first mask layer and an upper part of each third trench portion in the first mask layer have a cross section in a shape of a trapezoid with a decreasing width from top to bottom; and

forming word line structures in the second trench portions and the third trench portions.

2. The manufacturing method of the semiconductor structure according to claim 1,

wherein the second trench portion has a depth of 180 nm to 200 nm.

3. The manufacturing method of the semiconductor structure according to claim 1, wherein the third trench portion has a depth of 150 nm to 170 nm.

4. The manufacturing method of the semiconductor structure according to claim 1, wherein a difference between the width of the third trench portion and the width of the second trench portion is 1 nm to 5 nm.

5. The manufacturing method of the semiconductor structure according to any one of claims 1 to 4, wherein a material of the first mask layer comprises Si_3N_4.

6. The manufacturing method of the semiconductor structure according to any one of claims 1 to 5, wherein the first mask layer has a thickness of 15 nm to 30 nm.

7. The manufacturing method of the semiconductor structure according to any one of claims 1 to 6, wherein the first mask layer is formed by an atomic layer deposition process.

8. The manufacturing method of the semiconductor structure according to any one of claims 1 to 7, wherein the planarizing the first mask layer comprises:

planarizing the first mask layer by a chemical-mechanical polishing process.

9. The manufacturing method of the semiconductor structure according to any one of claims 1 to 8, wherein the removing part of the first mask layer, part of the isolation layer, and part of the substrate, to form a second trench comprising second trench portions and third trench portions arranged alternatively in a direction comprises:

forming a second mask layer on the first mask layer, wherein the second mask layer covers a surface of the first mask layer;

forming a patterned photoresist layer on the second mask layer; and

etching part of the first mask layer, part of the isolation layer, and part of the substrate by using the photoresist layer as a mask.

10. The manufacturing method of the semiconductor structure according to claim 9, wherein the forming a patterned photoresist layer on the second mask layer comprises:

forming a photoresist material layer on the second mask layer; and

removing part of the photoresist material layer by using an exposure and development technology, wherein the remaining part of photoresist material layer forms

the photoresist layer.

11. The manufacturing method of the semiconductor structure according to claim 9, wherein the etching part of the first mask layer, part of the isolation layer, and part of the substrate by using the photoresist layer as a mask comprises:

etching part of the second mask layer by using the photoresist layer as a mask, to form fourth trenches in the second mask layer;

removing the photoresist layer;

etching part of the first mask layer, part of the isolation layer, and part of the substrate downward along the fourth trenches; and

removing the second mask layer.

12. The manufacturing method of the semiconductor structure according to any one of claims 1 to 11, wherein the forming word line structures in the second trench portions and the third trench portions comprises:

forming a metal barrier material layer, wherein the metal barrier material layer covers an upper surface of the first mask layer, a bottom and sidewalls of each of the second trench portions and a bottom and sidewalls of each of the third trench portions;

forming a conductive material layer, wherein the conductive material layer covers a surface of the metal barrier material layer and fills the second trench portions and the third trench portions; and

removing part of the metal barrier material layer and part of the conductive material layer, wherein a remaining part of the metal barrier material layer is a barrier layer, and a remaining part of the conductive material layer is a conductive layer, the barrier layer and the conductive layer forming each of the word line structures;

wherein an upper surface of the barrier layer and an upper surface of the conductive layer are lower than an upper surface of each of the active regions.

13. The manufacturing method of the semiconductor structure according to claim 12, wherein

the upper surface of the barrier layer is lower than the upper surface of the conductive layer.

14. The manufacturing method of the semiconductor structure according to any

one of claims 1 to 13, after the forming word line structures in the second trench portions and the third trench portions, the method further comprises:

forming a protective layer, wherein the protective layer covers surfaces of the word line structures and fills the second trench portions and the third trench portions.

15. A semiconductor structure, comprising:

a substrate, comprising active regions and isolation regions, wherein each of the isolation regions comprises a first trench and an isolation layer formed in the first trench;

a first mask layer covering an upper surface of the isolation layer and upper surfaces of the active regions, wherein a whole upper surface of the isolation layer is lower than upper surfaces of the active regions;

a second trench comprising second trench portions and third trench portions arranged alternatively in a direction, wherein a lower part of each of the second trench portions is located in a respective one of the isolation regions, a lower part of each of the third trench portions is located in a respective one of the active regions, and a width of each third trench portion is greater than a width of each second trench portion, and an upper part of each second trench portion in the first mask layer and an upper part of each third trench portion in the first mask layer have a cross section in a shape of a trapezoid with a decreasing width from top to bottom; and

word line structures, wherein the word line structures are provided in the second trench portions and the third trench portions.

16. The semiconductor structure according to claim 15, wherein each of the word line structures comprise a barrier layer and a conductive layer, and an upper surface of the barrier layer and an upper surface of the conductive layer are lower than an upper surface of each of the active regions.

17. The semiconductor structure according to claim 16, further comprising:

a protective layer, wherein the protective layer covers surfaces of the word line structures and fills the second trench portions and the third trench portions.