Claims

1. A method for forming a device, comprising:

forming a film stack on a substrate, wherein the film stack comprises a plurality of alternating layers of oxide layers and nitride layers and has a stack thickness;

etching the film stack to a first depth to form a plurality of openings between a plurality of structures, wherein each structure has a sidewall and each opening has a bottom, wherein the first depth is less than the stack thickness, and wherein each opening has an aspect ratio of greater than 50 relative to the first depth;

depositing an etch protection liner comprising amorphous-silicon on the sidewalls and the bottoms;

removing the etch protection liner from at least the bottoms of the openings;

forming a plurality of holes by etching the film stack in the openings to further extend each bottom of the openings to a second depth of the hole; and

removing the etch protection liner from the sidewalls.

2. The method of claim 1, wherein each opening has an aspect ratio of greater than 100 to 500 relative to the first depth.

3. The method of claim 1, wherein a thickness of the etch protection liner deposited on the bottoms of the openings is less than a thickness of the etch protection liner deposited on the sidewalls of the structures.

4. The method of claim 1, wherein the etch protection liner is deposited by a thermal chemical vapor deposition (CVD) process.

5. The method of claim 4, wherein the thermal CVD process comprises exposing the sidewalls and the bottoms to a process gas comprising a silicon precursor selected from the group consisting of silane, disilane, trisilane, tetrasilane, and any combination thereof.

6. The method of claim 1, wherein the etch protection liner has a thickness of 1 nm to 50 nm.

7. The method of claim 1, wherein the etch protection liner has a thickness of 2 nm to 10 nm.

8. The method of claim 1, wherein the stack thickness is in a range of 1 µM to 10 µM.

9. The method of claim 1, wherein the plurality of alternating layers of oxide layers and nitride layers comprises 20 pairs to 200 pairs of oxide layers and nitride layers.

10. The method of claim 1, wherein each of the openings and each of the holes independently have a width of 1 nm to 3,000 nm.

11. The method of claim 1, wherein the second depth is in a range of 1 µM to 10 µM.

12. The method of claim 1, wherein each of the holes is a memory hole or a word line slit.

13. A method for forming a device, comprising:

forming a film stack on a substrate, wherein the film stack comprises a plurality of alternating layers of oxide layers and nitride layers and has a stack thickness;

forming a patterned hard mask on the film stack;

etching the film stack to a first depth to form a plurality of openings between a plurality of structures, wherein each structure has a sidewall and each opening has a bottom, wherein the first depth is less than the stack thickness, and wherein each opening has an aspect ratio of greater than 100 relative to the first depth;

depositing an etch protection liner comprising amorphous-silicon on the sidewalls and the bottoms by a thermal chemical vapor deposition (CVD) process, wherein the etch protection liner has a thickness of 1 nm to 50 nm;

removing the etch protection liner from at least the bottoms of the openings;

forming a plurality of holes by etching the film stack in the openings to further extend each bottom of the openings to a second depth of the hole; and

removing the etch protection liner from the sidewalls.

14. The method of claim 13, wherein each opening has an aspect ratio of 120 to 500 relative to the first depth.

15. The method of claim 13, wherein a thickness of the etch protection liner deposited on the bottoms of the openings is less than a thickness of the etch protection liner deposited on the sidewalls of the structures.

16. The method of claim 13, wherein the thermal CVD process comprises exposing the sidewalls and the bottoms to a process gas comprising a silicon precursor selected from the group consisting of silane, disilane, trisilane, tetrasilane, and any combination thereof.

17. The method of claim 13, wherein the etch protection liner has a thickness of 2 nm to 20 nm.

18. The method of claim 13, wherein each of the openings and each of the holes independently have a width of 1 nm to 3,000 nm.

19. The method of claim 13, wherein the second depth is in a range of 1 μM to 10 μM.

20. A microelectronic device, comprising:

a film stack disposed on a substrate, wherein the film stack comprises a plurality of alternating layers of oxide layers and nitride layers and has a stack thickness;

a patterned hard mask disposed on an upper surface of the film stack;

a plurality of openings having a first depth disposed between a plurality of structures, wherein each structure has a sidewall and each opening has a bottom,

wherein the first depth is less than the stack thickness, and wherein each opening has an aspect ratio of greater than 100 relative to the first depth; and

an etch protection liner comprising amorphous-silicon disposed on the patterned hard mask, the sidewalls, and the bottoms, wherein the etch protection liner has a thickness of 1 nm to 50 nm.