addressing military and civilian requirements for communications between individuals, electronic devices, control centers, and electronic systems for example.

[005] Accordingly, it would be beneficial for UWB transmitters, UWB receivers and UWB transceivers to accommodate and adapt to what are commonly referred to as inaccuracies, errors, or issues within the implemented electronics, hardware, firmware, and software.

[006] Accordingly, it would be beneficial for receivers to accommodate offsets in absolute frequency between their frequency source and that within the transmitter.

[007] It would be further beneficial for the UWB radios to employ modulation coding schemes that are more efficient with respect to power, data bits per pulse transmitted, and enabled operation at higher output power whilst complying with regulatory emission requirements.

[008] It would be further beneficial for the UWB receivers to accommodate drift within their own electronics arising from phase locked loop and/or from relative clock frequency offsets of the remote transmitter and local receiver.

[009] It would be further beneficial for UWB devices to support a ranging function over a range and with an accuracy that are not limited by the low frequency master clock employed within these devices to enable their operation with ultra-low power consumption.

[0010] Other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

SUMMARY OF THE INVENTION

[0011] It is an object of the present invention to mitigate limitations within the prior art relating to ultra-wideband wireless communication systems and more particularly ultra-wideband receivers for such ultra-wideband wireless communication systems.

[0011a] Aspects of the invention are defined in the independent claims. Embodiments or preferred/optional features are defined in the dependent claims.

[0012] In accordance with an embodiment of the invention there is provided a UWB receiver comprising:

an antenna for receiving wireless signals coupled to a signal processing circuit; and

the signal processing circuit comprising:

an RF front end circuit comprising:

CLAIMS

What is claimed is:

1. A wireless receiver comprising:

a digital processor configured to execute a process; and

an energy based detector configured to process first data received by the wireless receiver from which second data is decoded where the energy based detector employs an integration circuit configured to provide integration within an integration window of a plurality of integration windows and an analog-to-digital converter (ADC) configured to convert an output of the integration circuit; wherein

for executing the process, the digital processor is configured to:

process analog-to-digital converter (ADC) code values of N last '0's within the received first data for a first integration window of the plurality of integration windows and ADC code values of the N last '1's within the received first data for the first integration window of the plurality of integration windows to generate a first coarse metric of a first received signal-to-noise ratio for the first integration window of the plurality of integration windows;

process the analog-to-digital converter (ADC) code values of N last '0's within the received first data for a second integration window of the plurality of integration windows and the ADC code values of the N last '1's within the received first data for the second integration window of the plurality of integration windows to establish a second coarse metric of a second received signal-to-noise ratio for the second integration window of the plurality of integration windows, the second integration window of the plurality of integration windows being an integration window of the plurality of integration windows immediately prior to the first integration window of the plurality of integration windows;

process the analog-to-digital converter (ADC) code values of N last '0's within the received first data for a third integration window of the plurality of integration windows and the ADC code values of the N last '1's within the received first data for the third integration window of the plurality of integration windows to establish a third coarse metric of a third received signal-to-noise ratio for the third integration window of the plurality of integration windows, the third

integration window of the plurality of integration windows being an immediately subsequent integration window of the plurality of integration windows to the first integration window of the plurality of integration windows;

establish in dependence upon the first coarse metric of the first received signal-to-noise ratio for the first integration window of the plurality of integration windows, the second coarse metric of the second received signal-to-noise ratio for the second integration window of the plurality of integration windows, and the third coarse metric of the third received signal-to-noise ratio for the third integration window of the plurality of integration windows a current integration window for the energy based detector from the first integration window of the plurality of integration windows, the second integration window of the plurality of integration windows and the third integration window of the plurality of integration windows; and

N is a positive integer greater than or equal to 2.

2. The wireless receiver according to claim 1, wherein the wireless receiver is configured for the second integration window of the plurality of integration windows to overlap a first portion of the first integration window of the plurality of integration windows and the third integration window of the plurality of integration windows to overlap a second portion of the first integration window of the plurality of integration windows.

3. The wireless receiver according to claim 1, wherein, for processing the ADC code values of the N last '0's and the ADC code values of the N last '1's, the digital processor is configured to either subtract the ADC code values of the N last ‘0’s from the ADC code values of the N last ‘1’s or ignore the ADC code values of the N last ‘0’s.

4. The wireless receiver according to claim 1, wherein the digital processor is configured to dynamically set the value of N in dependence upon at least one of a packet size of packets comprising the first data, a rate of clock drift established in dependence upon the timing of shifting integration windows within the plurality of integration windows and a measure of an overall signal SNR for the received first data.