ENERGY RECOVERY ADIABATIC FLIP-FLOP AND RESONATOR BASED BENNETT CLOCK GENERATOR

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Patent Application No. 63/354,109, filed June 21, 2022, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] Despite the exponential progress over the past fifty years the increase of performance of computing devices is coming to an end. Modern microprocessors are limited by heat generation, and their speeds have been capped at 4 GHz since 2004. Traditional Complementary MOSFET logic (CMOS) circuits dissipate energy every time they switch in the form of heat.

[0003] Accordingly, those skilled in the art continue research and development in the field of energy recovery for computing devices.

SUMMARY

[0003a] In an aspect, the present disclosure refers to a method comprising:

during a time period A, in a computer storage element having first and second power inputs separated by an array of transistors of the computer storage element configured for storing a computer bit of data, moving an input of the array of transistors a logic value “1” or “0” to a master latch;

during a time period B, after time period A, recovering at least a portion of energy comprising the input with a first clock;

during a time period C, after time period B, moving the input in the master latch to an isolation stage;

during a time period D, after time period C, recovering at least a portion of energy comprising the input from the isolation stage with a second clock;

during a time period E, after time period D, recovering at least a portion of energy comprising the input from a follower latch with a third clock; and

during a time period F, after time period E, moving at least a portion of the input from the isolation stage to the follower latch.

[0004] Generally, provided, in some non-limiting embodiments or examples, is a computer storage element and method of use thereof. In some non-limiting embodiments, the computer storage element may be a flip-flop or memory. In some non-limiting embodiments, the computer storage element may be operated in a manner that reduces, minimizes, or avoids electrical power from entering the computer storage element and thereby power consumption and, hence, heat generation in the computer storage element over prior methods of use.

[0005] In one example, the disclosed method includes during a time period A, in a computer storage element having first and second power inputs separated by an array of transistors of the computer storage element configured for storing a computer bit of data, moving an input of the array of transistors a logic value “1” or “0” to a master latch., during a time period B, after time period A, recovering at least a portion of energy comprising the input with a first clock, during a time period C, after time period B, moving the input in the master latch to an isolation stage, during a time period D, after time period C, recovering at least a portion of energy comprising the input from the isolation stage with a second clock, during a time period E, after time period D, recovering at least a portion of energy comprising the input from a follower latch with a third clock, and during a time period F, after time period E, moving at least a portion of the input from the isolation stage to the follower latch.