WHAT IS CLAIMED IS:

1. A memory apparatus, comprising:

a first transistor region of an integrated circuit cell structure, the first transistor region having a first active region and a second active region in parallel with a first distance separating the first and second active regions;

a second transistor region of the integrated circuit cell structure, the second transistor region having a third active region and a fourth active region in parallel with a second distance separating the third and fourth active regions, wherein at least a portion of the second transistor region is positioned below the first transistor region in a vertical dimension of the integrated circuit cell structure, and wherein the second transistor region is complementary to the first transistor region;

a first inverter including:

a first transistor with a first gate formed in the first active region, the first gate having a first source/drain region and a second source/drain region on opposing sides of the first gate; and

a second transistor with a second gate formed in the third active region, the second gate having a third source/drain region and a fourth source/drain region on opposing sides of the second gate, wherein the third source/drain region is merged with the first source/drain region and the fourth source/drain region is merged with the second source/drain region, and wherein a portion of the second gate extends below the first transistor region;

a second inverter including:

a third transistor with a third gate formed in the second active region, the third gate having a fifth source/drain region and a sixth source/drain region on opposing sides of the third gate; and

a fourth transistor with a fourth gate formed in the fourth active region, the fourth gate having a seventh source/drain region and an eighth source/drain region on opposing sides of the fourth gate, wherein the seventh source/drain region is merged with the fifth source/drain region and the eighth source/drain region is merged with the sixth source/drain region,

and wherein a portion of the fourth gate extends below the first transistor region;

wherein the first inverter is cross-coupled to the second inverter by a first coupling between the portion of the second gate that extends below the second active region and the seventh source/drain region and a second coupling between the portion of the fourth gate that extends below the first active region and the fourth source/drain region, the first coupling and the second coupling being positioned below the second transistor region in the vertical dimension.

2. The memory apparatus of claim 1, further comprising a first pass gate coupled to a wordline, the first pass gate being formed in the second active region and having the fifth source/drain region and a ninth source/drain region on opposing sides of the first pass gate, wherein the ninth source/drain region is coupled to a first bitline.

3. The memory apparatus of claim 2, wherein the portion of the second gate that extends below the first transistor region is positioned below the first pass gate.

4. The memory apparatus of claim 2, further comprising a second pass gate coupled to the wordline, the second pass gate being formed in the first active region and having the second source/drain region and a tenth source/drain region on opposing sides of the second pass gate, wherein the tenth source/drain region is coupled to a second bitline, the second bitline being complementary to the first bitline.

5. The memory apparatus of claim 4, wherein the portion of the fourth gate that extends below the first transistor region is positioned below the second pass gate.

6. The memory apparatus of claim 1, further comprising a metal layer located below the second transistor region in the vertical dimension, wherein the metal layer includes power routing connected to the first inverter and the second inverter.

7. The memory apparatus of claim 6, further comprising:

a first backside via coupling the power routing in the metal layer to the third source/drain region; and

a second backside via coupling the power routing in the metal layer to the eight source/drain region.

8. The memory apparatus of claim 1, further comprising a metal layer located above the first transistor region in the vertical dimension, wherein the metal layer includes signal routing connected to the first inverter and the second inverter.

9. The memory apparatus of claim 1, wherein the first inverter is cross-coupled to the second inverter such that an output of the first inverter is provided as input to the second inverter and an output of the second inverter is provided as input to the first inverter.

10. The memory apparatus of claim 1, wherein the third active region is positioned below the first active region and the fourth active region is positioned below the second active region.

11. The memory apparatus of claim 1, wherein the first distance is substantially the same as the second distance.

12. The memory apparatus of claim 1, wherein the portion of the second gate that extends below the first transistor region extends to an inactive portion of the fourth active region.

13. The memory apparatus of claim 1, wherein the portion of the fourth gate that extends below the first transistor region extends to an inactive portion of the third active region.

14. The memory apparatus of claim 13, wherein the inactive portion of the third active region has no diffusion material.

15. The memory apparatus of claim 1, further comprising:
a first gate merge via coupling the first gate and the second gate; and
a second gate merge via coupling the third gate and the fourth gate.

16. A memory apparatus, comprising:

a first transistor region of an integrated circuit cell structure, the first transistor region having a first active region and a second active region in parallel with a first distance separating the first and second active regions;

a second transistor region of the integrated circuit cell structure, the second transistor region having a third active region and a fourth active region in parallel with a second distance separating the third and fourth active regions, wherein at least a portion of the second transistor region is positioned below the first transistor region in a vertical dimension of the integrated circuit cell structure, and wherein the second transistor region is complementary to the first transistor region;

a first pass gate formed in the second active region, the first pass gate being coupled to a wordline, wherein a source/drain region of the first pass gate is coupled to a first bitline;

a second pass gate formed in the first active region, the second pass gate being coupled to the wordline, wherein a source/drain region of the second pass gate is coupled to a second bitline that is complementary to the first bitline;

a first inverter formed by a first transistor in the first active region and a second transistor in the third active region, wherein inputs of the first transistor and the second transistor are merged, wherein outputs of the first transistor and the second transistor are merged, and wherein a portion of the second transistor extends below the first pass gate in the vertical dimension;

a second inverter formed by a third transistor in the second active region and a fourth transistor in the fourth active region, wherein inputs of the third transistor and the fourth transistor are merged, wherein outputs of the third transistor and the fourth transistor are merged, and wherein a portion of the fourth transistor extends below the second pass gate in the vertical dimension;

a first coupling between the portion of the second transistor that extends below the first pass gate and a source/drain region of the fourth transistor, the first coupling being positioned below the second transistor region in the vertical dimension; and

a second coupling between the portion of the fourth transistor that extends below the second pass gate and a source/drain region of the second transistor, the second coupling being positioned below the second transistor region in the vertical dimension.

17. The memory apparatus of claim 16, wherein the first inverter is cross-coupled to the second inverter by the first coupling and the second coupling.

18. The memory apparatus of claim 16, further comprising a metal layer located below the second transistor region in the vertical dimension, wherein the metal layer includes power routing connected to the first inverter and the second inverter.

19. The memory apparatus of claim 18, wherein the first coupling and the second coupling are positioned between the metal layer and the second transistor region in the vertical dimension.

20. The memory apparatus of claim 16, wherein the outputs of the third transistor and the fourth transistor are provided as the inputs of the first transistor and the second transistor, and wherein the outputs of the first transistor and the second transistor are provided as the inputs of the third transistor and the fourth transistor.