WE CLAIM:

1. A fiber array for edge coupling of at least one optical fiber with at least one wafer substrate at an edge of the fiber array, the fiber array comprising:

an optical fiber core;

a fiber cladding having an edge, a top and a bottom, and covering the optical fiber core;

a V-groove mounted at the top of the fiber cladding; and

a fiber array lid at the bottom of the fiber cladding;

wherein the fiber cladding has a uniform cross section adjacent the edge, the fiber array lid as a taper adjacent the edge, and the V-groove has a uniform cross-section adjacent the edge.

2. The fiber array of claim 1, wherein the optical fiber core is single mode optical fiber core having a uniform cross section adjacent the edge of the fiber cladding.

3. The fiber array of claim 1, wherein the fiber array lid comprises a polymer.

4. The fiber array of claim 1, wherein an angle of the taper of the fiber array lid is 30° to 45°.

5. A photonic integrated circuit comprising:
a wafer substrate;
a fiber array according to claim 1 edge coupled to the wafer substrate.

6. The photonic integrated circuit of claim 5, wherein the optical fiber core is single mode.

7. The photonic integrated circuit of claim 5, wherein the optical fiber core is multimode.

8. The photonic integrated circuit of claim 5, wherein an angle of the taper of the fiber array lid is 30° to 45°.

9. The photonic integrated circuit of claim 6, wherein V-groove arrays are fabricated on separate silicon sub-mounts and are then edge coupled to the wafer substrate by active alignment.

10. The photonic integrated circuit of claim 5, wherein the wafer substrate comprises a deep trench structure, and the fiber array is aligned above the deep trench structure, the alignment including angle and position of the fiber array lid, wherein the angle of the fiber array lid is predetermined by a depth of the deep trench structure.

11. A method of manufacturing the photonic integrated circuit of claim 10, the method comprising;

a) a step of etching a silicon substrate of the wafer substrate to form the deep trench structure such that the deep trench structure forms the optical interface for edge coupling;
b) a step of performing a first polishing of the fiber array lid to form a polished fiber array lid aligned with the wafer substrate and above the deep trench structure;
c) a step of performing a second polishing of the above polished fiber array lid to place a further polished fiber array lid in proximity with an optical interface on the silicon substrate; and
d) the fiber core is adjusted in proximity with the silicon oxide substrate to achieve optical interconnection between the fiber array and the wafer substrate.

12. The method of claim 11, wherein an angle of the taper of the further polished fiber array lid is 30° to 45°.