CLAIMS

1. A physical layer protocol data unit PPDU-based communication method, wherein the method comprises:

generating a PPDU based on a mapping relationship between a data symbol and a chip sequence, wherein a length of each chip sequence is L, a minimum Hamming distance is greater than or equal to L/2, L is a positive integer, a bit length corresponding to a data symbol is less than a bit length of a chip sequence, and the minimum Hamming distance indicates a smallest Hamming distance between any two different chip sequences; and

sending the PPDU.

2. A physical layer protocol data unit PPDU communication method, wherein the method comprises:

receiving a PPDU; and

processing the PPDU based on a mapping relationship between a data symbol and a chip sequence, wherein a length of each chip sequence is L, a minimum Hamming distance is greater than or equal to L/2, L is a positive integer, a bit length corresponding to a data symbol is less than a bit length of a chip sequence, and the minimum Hamming distance indicates a smallest Hamming distance between any two different chip sequences.

3. The method according to claim 2, wherein the processing the PPDU based on a mapping relationship between a data symbol and a chip sequence comprises:

obtaining a first sequence in the PPDU, wherein a length of the first sequence is L;

determining, based on N chip sequences comprised in the mapping relationship between a data symbol and a chip sequence, a first chip sequence corresponding to the first sequence, wherein the first chip sequence is one of the N chip sequences, and N is a positive integer;

determining, based on the mapping relationship between a data symbol and a chip sequence, a data symbol corresponding to the first chip sequence; and

determining, based on the data symbol corresponding to the first chip sequence, an information bit corresponding to the first chip sequence.

4. The method according to any one of claims 1 to 3, wherein L=32, L=16, or L=8.

5. The method according to any one of claims 1 to 4, wherein the chip sequence is obtained based on at least one of the following:

[1 1 –1 –1 –1 –1 –1 –1] and [1 1 –1 1 –1 1 –1 –1];

[1 –1 1 –1 –1 –1 –1 –1] and [1 1 –1 1 1 –1 –1 –1]; and

[1 –1 –1 1 –1 –1 –1 –1] and [1 1 1 –1 1 –1 –1 –1].

6. The method according to any one of claims 1 to 5, wherein the chip sequence is obtained

based on at least two of the following:

$$[\,1 \quad 1 \quad -1 \quad 1 \quad -1 \quad 1 \quad -1 \quad -1\,]$$
$$[\,1 \quad 1 \quad -1 \quad 1 \quad 1 \quad -1 \quad -1 \quad -1\,]\,.$$
$$[\,1 \quad 1 \quad 1 \quad -1 \quad 1 \quad -1 \quad -1 \quad -1\,]$$

7. The method according to any one of claims 1 to 4, wherein the chip sequence is obtained based on a Hadamard matrix, and an order of the Hadamard matrix is related to the length of the chip sequence.

8. The method according to claim 7, wherein at least two columns of elements in a matrix formed by the chip sequence are the same.

9. The method according to any one of claims 1 to 4, wherein the chip sequence is obtained based on the following two sequences:

[1 0 0 1 0 1 1 0 1 1 1 1 0 1 0 1 0 0 0 1 0 0 1 1 1 0 0 0 0 0 1]; and

[0 0 0 1 1 1 0 1 0 1 0 0 1 0 1 1 1 1 0 0 1 1 0 1 1 0 0 0 0 0 1].

10. The method according to claim 5 or 6, wherein the mapping relationship between a data symbol and a chip sequence is as follows:

Data symbol	Chip sequence
0	1 1 1 1 0 1 0 0 0 1 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1 0 1 0 1 0 0 1
1	1 0 0 1 1 1 1 1 0 1 0 0 0 1 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1 0 1 0
2	1 0 1 0 1 0 0 1 1 1 1 1 0 1 0 0 0 1 0 0 1 1 0 1 0 1 1 0 0 1 1 1
3	0 1 1 1 1 0 1 0 1 0 0 1 1 1 1 1 0 1 0 0 0 1 0 0 1 1 0 1 0 1 1 0
4	0 1 1 0 0 1 1 1 1 0 1 0 1 0 0 1 1 1 1 1 1 0 1 0 0 0 1 0 0 1 1 0 1
5	1 1 0 1 0 1 1 0 0 1 1 1 1 0 1 0 1 0 0 1 1 1 1 1 1 0 1 0 0 0 1 0 0
6	0 1 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1 0 1 0 1 0 0 1 1 1 1 1 1 0 1 0 0
7	0 1 0 0 0 1 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1 0 1 0 1 0 0 1 1 1 1 1
8	1 0 1 0 0 0 0 1 0 0 0 1 1 0 0 0 0 0 1 1 0 0 1 0 1 1 1 1 1 1 0 0
9	1 1 0 0 1 0 1 0 0 0 0 1 0 0 0 1 1 0 0 0 0 0 1 1 0 0 1 0 1 1 1 1
10	1 1 1 1 1 1 0 0 1 0 1 0 0 0 0 1 0 0 0 1 1 0 0 0 0 0 1 1 0 0 1 0
11	0 0 1 0 1 1 1 1 1 1 0 0 1 0 1 0 0 0 0 1 0 0 0 1 1 0 0 0 0 0 1 1
12	0 0 1 1 0 0 1 0 1 1 1 1 1 1 0 0 1 0 1 0 0 0 0 1 0 0 0 1 1 0 0 0
13	1 0 0 0 0 0 1 1 0 0 1 0 1 1 1 1 1 1 0 0 1 0 1 0 0 0 0 1 0 0 0 1
14	0 0 0 1 1 0 0 0 0 0 1 1 0 0 1 0 1 1 1 1 1 1 0 0 1 0 1 0 0 0 0 1
15	0 0 0 1 0 0 0 1 1 0 0 0 0 0 1 1 0 0 1 0 1 1 1 1 1 1 0 0 1 0 1 0

11. The method according to claim 5 or 6, wherein the mapping relationship between a data symbol and a chip sequence is as follows:

Data symbol	Chip sequence
0	1 1 1 1 1 0 1 1 0 0 1 1 1 1 0 1 0 0 0 0 1 0 0 1 0 1 1 0 0 1 0 1
1	0 1 0 1 1 1 1 1 1 0 1 1 0 0 1 1 1 1 0 1 0 0 0 0 1 0 0 1 0 1 1 0
2	0 1 1 0 0 1 0 1 1 1 1 1 1 0 1 1 0 0 1 1 1 1 0 1 0 0 0 0 1 0 0 1
3	1 0 0 1 0 1 1 0 0 1 0 1 1 1 1 1 1 0 1 1 0 0 1 1 1 1 0 1 0 0 0 0
4	0 0 0 0 1 0 0 1 0 1 1 0 0 1 0 1 1 1 1 1 1 0 1 1 0 0 1 1 1 1 0 1
5	1 1 0 1 0 0 0 0 1 0 0 1 0 1 1 0 0 1 0 1 1 1 1 1 1 0 1 1 0 0 1 1
6	0 0 1 1 1 1 0 1 0 0 0 0 1 0 0 1 0 1 1 0 0 1 0 1 1 1 1 1 1 0 1 1
7	1 0 1 1 0 0 1 1 1 1 0 1 0 0 0 0 1 0 0 1 0 1 1 0 0 1 0 1 1 1 1 1
8	1 0 1 0 1 1 1 0 0 1 1 0 1 0 0 0 0 1 0 1 1 1 0 0 0 0 1 1 0 0 0 0
9	0 0 0 0 1 0 1 0 1 1 1 0 0 1 1 0 1 0 0 0 0 1 0 1 1 1 0 0 0 0 1 1
10	0 0 1 1 0 0 0 0 1 0 1 0 1 1 1 0 0 1 1 0 1 0 0 0 0 1 0 1 1 1 0 0
11	1 1 0 0 0 0 1 1 0 0 0 0 1 0 1 0 1 1 1 0 0 1 1 0 1 0 0 0 0 1 0 1
12	0 1 0 1 1 1 0 0 0 0 1 1 0 0 0 0 1 0 1 0 1 1 1 0 0 1 1 0 1 0 0 0
13	1 0 0 0 0 1 0 1 1 1 0 0 0 0 1 1 0 0 0 0 1 0 1 0 1 1 1 0 0 1 1 0
14	0 1 1 0 1 0 0 0 0 1 0 1 1 1 0 0 0 0 1 1 0 0 0 0 1 0 1 0 1 1 1 0
15	1 1 1 0 0 1 1 0 1 0 0 0 0 1 0 1 1 1 0 0 0 0 1 1 0 0 0 0 1 0 1 0

12. The method according to claim 5 or 6, wherein the mapping relationship between a data symbol and a chip sequence is as follows:

Data symbol	Chip sequence
0	1 1 1 0 0 0 0 1 1 1 0 0 0 0 1 0 1 1 1 1 0 1 1 1 0 1 1 1 1 1 1 0
1	1 1 1 0 1 1 1 0 0 0 0 1 1 1 0 0 0 0 1 0 1 1 1 1 0 1 1 1 0 1 1 1
2	0 1 1 1 1 1 1 0 1 1 1 0 0 0 0 1 1 1 0 0 0 0 1 0 1 1 1 1 0 1 1 1
3	0 1 1 1 0 1 1 1 1 1 1 0 1 1 1 0 0 0 0 1 1 1 0 0 0 0 1 0 1 1 1 1
4	1 1 1 1 0 1 1 1 0 1 1 1 1 1 1 0 1 1 1 0 0 0 0 1 1 1 0 0 0 0 1 0
5	0 0 1 0 1 1 1 1 0 1 1 1 0 1 1 1 1 1 1 0 1 1 1 0 0 0 0 1 1 1 0 0
6	1 1 0 0 0 0 1 0 1 1 1 1 0 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 0 0 0 0 1
7	0 0 0 1 1 1 0 0 0 0 1 0 1 1 1 1 0 1 1 1 0 1 1 1 1 1 1 1 0 1 1 1 0
8	1 0 1 1 0 1 0 0 1 0 0 1 0 1 1 1 1 0 1 0 0 0 1 0 0 0 1 0 1 0 1 1
9	1 0 1 1 1 0 1 1 0 1 0 0 1 0 0 1 0 1 1 1 1 0 1 0 0 0 1 0 0 0 1 0
10	0 0 1 0 1 0 1 1 1 0 1 1 0 1 0 0 1 0 0 1 0 1 1 1 1 0 1 0 0 0 1 0
11	0 0 1 0 0 0 1 0 1 0 1 1 1 0 1 1 0 1 0 0 1 0 0 1 0 1 1 1 1 0 1 0
12	1 0 1 0 0 0 1 0 0 0 1 0 1 0 1 1 1 0 1 1 0 1 0 0 1 0 0 1 0 1 1 1

Data symbol	Chip sequence
13	0 1 1 1 1 0 1 0 0 0 1 0 0 0 1 0 1 0 1 1 1 0 1 1 0 1 0 0 1 0 0 1
14	1 0 0 1 0 1 1 1 1 0 1 0 0 0 1 0 0 0 1 0 1 0 1 1 1 0 1 1 0 1 0 0
15	0 1 0 0 1 0 0 1 0 1 1 1 1 0 1 0 0 0 1 0 0 0 1 0 1 0 1 1 1 0 1 1

13. The method according to any one of claims 1 to 4, or 7, wherein the mapping relationship between a data symbol and a chip sequence is as follows:

Data symbol	Chip sequence
0	1 1 0 0 1 0 1 0 1 0 0 1 0 0 0 0 1 1 0 0 1 0 1 0 0 1 1 0 1 1 1 1
1	1 0 1 0 1 1 0 0 1 1 1 1 0 1 1 0 1 0 1 0 1 1 0 0 0 0 0 0 1 0 0 1
2	1 0 0 1 0 0 0 0 1 1 0 0 1 0 1 0 1 0 0 1 0 0 0 0 0 0 1 1 0 1 0 1
3	1 1 1 1 0 1 1 0 1 0 1 0 1 1 0 0 1 1 1 1 0 1 1 0 0 1 0 1 0 0 1 1
4	1 0 0 1 1 1 1 1 0 0 1 1 1 0 1 0 1 0 0 1 1 1 1 1 1 1 0 0 0 1 0 1
5	1 1 1 1 1 0 0 1 0 1 0 1 1 1 0 0 1 1 1 1 1 0 0 1 1 0 1 0 0 0 1 1
6	1 1 0 0 0 1 0 1 0 1 1 0 0 0 0 0 1 1 0 0 0 1 0 1 1 0 0 1 1 1 1 1
7	1 0 1 0 0 0 1 1 0 0 0 0 0 1 1 0 1 0 1 0 0 0 1 1 1 1 1 1 1 0 0 1
8	1 0 0 1 1 1 1 1 1 1 0 0 0 1 0 1 0 1 1 0 0 0 0 0 1 1 0 0 0 1 0 1
9	1 1 1 1 1 0 0 1 1 0 1 0 0 0 1 1 0 0 0 0 0 1 1 0 1 0 1 0 0 0 1 1
10	1 1 0 0 0 1 0 1 1 0 0 1 1 1 1 1 0 0 1 1 1 0 1 0 1 0 0 1 1 1 1 1
11	1 0 1 0 0 0 1 1 1 1 1 1 1 1 0 0 1 0 1 0 1 1 1 0 0 1 1 1 1 1 0 0 1
12	1 1 0 0 1 0 1 0 0 1 1 0 1 1 1 1 0 0 1 1 0 1 0 1 0 1 1 0 1 1 1 1
13	1 0 1 0 1 1 0 0 0 0 0 0 1 0 0 1 0 1 0 1 0 0 1 1 0 0 0 0 1 0 0 1
14	1 0 0 1 0 0 0 0 0 0 1 1 0 1 0 1 0 1 1 0 1 1 1 1 0 0 1 1 0 1 0 1
15	1 1 1 1 0 1 1 0 0 1 0 1 0 0 1 1 0 0 0 0 1 0 0 1 0 1 0 1 0 0 1 1

14. The method according to claim 9, wherein the mapping relationship between a data symbol and a chip sequence is as follows:

Data symbol	Chip sequence
0	1 0 0 1 1 1 0 1 0 1 1 0 0 0 1 1 0 0 0 1 0 1 0 0 0 1 0 0 0 1 0 0
1	1 0 1 0 1 0 1 1 0 1 1 1 1 1 1 1 1 0 0 1 0 0 1 0 1 1 1 1 1 0 0 1
2	1 1 1 1 0 0 1 0 1 0 1 0 1 1 0 1 1 1 1 1 1 1 1 1 0 0 1 0 0 1 0 1 1
3	0 1 1 1 1 0 0 1 0 1 0 1 0 1 1 0 1 1 1 1 1 1 1 1 0 0 1 0 0 1 0 1
4	1 0 1 0 1 1 1 1 1 0 0 1 0 1 0 1 0 1 1 0 1 1 1 1 1 1 1 1 0 0 1 0
5	1 1 0 0 0 0 0 1 0 0 0 0 1 0 0 1 0 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0

Data symbol	Chip sequence
6	1 0 1 0 0 0 0 0 1 0 0 0 0 1 0 0 1 0 0 1 0 0 1 1 1 0 0 1 0 1 1 1
7	1 0 1 1 1 0 1 0 0 0 0 0 1 0 0 0 0 1 0 0 1 0 0 1 0 0 1 1 1 0 0 1
8	0 1 1 0 0 1 0 1 1 1 0 1 0 0 0 0 0 1 0 0 0 0 1 0 0 1 0 0 1 0 0 1
9	0 0 0 1 0 1 0 0 0 1 1 1 1 0 0 0 1 0 0 0 1 1 1 1 1 1 1 0 0 0 1 1
10	0 1 0 1 0 0 1 1 1 1 0 0 1 1 0 0 1 1 0 0 0 1 0 0 1 1 1 1 0 1 0 0
11	0 0 1 0 0 1 0 0 0 1 1 0 1 1 1 0 0 1 1 0 1 1 1 0 1 0 0 1 1 1 0 0
12	1 1 0 1 1 1 0 0 1 1 0 1 1 1 0 1 0 0 1 1 1 0 0 0 1 0 0 1 0 0 0 1
13	0 0 0 0 0 0 1 1 1 0 1 1 0 0 1 0 0 0 1 1 1 0 0 0 0 0 0 1 1 0 1 0
14	0 1 0 1 1 0 0 0 0 0 1 1 0 1 1 1 1 1 0 0 0 1 0 1 1 0 0 1 1 0 1 0
15	0 1 1 0 1 1 0 0 1 1 0 0 1 0 1 1 1 1 0 1 1 0 0 1 1 1 1 1 0 1 1 1 0

15. The method according to any one of claims 1 to 4, wherein the mapping relationship between a data symbol and a chip sequence is as follows:

Data symbol	Chip sequence
0	1 0 1 1 0 1 1 0 1 1 0 0 0 1 0 0
1	0 0 1 0 1 1 0 1 1 0 1 1 0 0 0 1
2	0 1 0 0 1 0 1 1 0 1 1 0 1 1 0 0
3	0 0 0 1 0 0 1 0 1 1 0 1 1 0 1 1
4	1 1 0 0 0 1 0 0 1 0 1 1 0 1 1 0
5	1 0 1 1 0 0 0 1 0 0 1 0 1 1 0 1
6	0 1 1 0 1 1 0 0 0 1 0 0 1 0 1 1
7	1 1 0 1 1 0 1 1 0 0 0 1 0 0 1 0
8	1 1 1 0 0 0 1 1 1 0 0 1 0 0 0 1
9	0 1 1 1 1 0 0 0 1 1 1 0 0 1 0 0
10	0 0 0 1 1 1 1 0 0 0 1 1 1 0 0 1
11	0 1 0 0 0 1 1 1 1 0 0 0 1 1 1 0
12	1 0 0 1 0 0 0 1 1 1 1 0 0 0 1 1
13	1 1 1 0 0 1 0 0 0 1 1 1 1 0 0 0
14	0 0 1 1 1 0 0 1 0 0 0 1 1 1 1 0
15	1 0 0 0 1 1 1 0 0 1 0 0 0 1 1 1

16. The method according to any one of claims 1 to 4, wherein the mapping relationship between a data symbol and a chip sequence is as follows:

Data symbol	Chip sequence
0	1 1 0 1 1 0 0 0
1	1 0 0 0 0 0 1 0
2	1 0 1 1 1 1 1 0
3	1 1 1 0 0 1 0 0
4	1 0 1 1 0 0 0 1
5	1 1 1 0 1 0 1 1
6	1 1 0 1 0 1 1 1
7	1 0 0 0 1 1 0 1
8	1 1 0 1 1 0 0 0
9	1 0 0 0 0 0 1 0
10	1 0 1 1 1 1 1 0
11	1 1 1 0 0 1 0 0
12	1 0 1 1 0 0 0 1
13	1 1 1 0 1 0 1 1
14	1 1 0 1 0 1 1 1
15	1 0 0 0 1 1 0 1

17. A communication apparatus, wherein the apparatus comprises:

a processing unit, configured to generate a PPDU based on a mapping relationship between a data symbol and a chip sequence, wherein a length of each chip sequence is L, a minimum Hamming distance is greater than or equal to L/2, L is a positive integer, a bit length corresponding to the data symbol is less than a bit length of a chip sequence, and the minimum Hamming distance indicates a smallest Hamming distance between any two different chip sequences; and

a transceiver unit, configured to send the PPDU.

18. A communication apparatus, wherein the apparatus comprises:

a transceiver unit, configured to receive a PPDU; and

a processing unit, configured to process the PPDU based on a mapping relationship between a data symbol and a chip sequence, wherein a length of each chip sequence is L, a minimum Hamming distance is greater than or equal to L/2, L is a positive integer, a bit length corresponding to the data symbol is less than a bit length of a chip sequence, and the minimum Hamming distance indicates a smallest Hamming distance between any two different chip sequences.

19. The apparatus according to claim 18, wherein the processing unit is specifically configured to: obtain a first sequence in the PPDU, wherein a length of the first sequence is L; determine, based on N chip sequences comprised in the mapping relationship between a data

symbol and a chip sequence, a first chip sequence corresponding to the first sequence, wherein the first chip sequence is one of the N chip sequences, and N is a positive integer; determine, based on the mapping relationship between a data symbol and a chip sequence, a data symbol corresponding to the first chip sequence; and determine, based on the data symbol corresponding to the first chip sequence, an information bit corresponding to the first chip sequence.

20. The apparatus according to any one of claims 17 to 19, wherein L=32, L=16, or L=8.

21. The apparatus according to any one of claims 17 to 20, wherein the chip sequence is obtained based on at least one of the following:

[1 1 –1 –1 –1 –1 –1 –1] and [1 1 –1 1 –1 1 –1 –1];

[1 –1 1 –1 –1 –1 –1 –1] and [1 1 –1 1 1 –1 –1 –1]; and

[1 –1 –1 1 –1 –1 –1 –1] and [1 1 1 –1 1 –1 –1 –1].

22. The apparatus according to any one of claims 17 to 21, wherein the chip sequence is obtained based on at least two of the following:

$$\begin{bmatrix} 1 & 1 & -1 & 1 & -1 & 1 & -1 & -1 \\ 1 & 1 & -1 & 1 & 1 & -1 & -1 & -1 \\ 1 & 1 & 1 & -1 & 1 & -1 & -1 & -1 \end{bmatrix}.$$

23. The apparatus according to any one of claims 17 to 20, wherein the chip sequence is obtained based on a Hadamard matrix, and an order of the Hadamard matrix is related to the length of the chip sequence.

24. The apparatus according to any one of claims 17 to 20, or 23, wherein the mapping relationship between a data symbol and a chip sequence is as follows:

Data symbol	Chip sequence
0	1 1 0 0 1 0 1 0 1 0 0 1 0 0 0 0 1 1 0 0 1 0 1 0 0 1 1 0 1 1 1 1
1	1 0 1 0 1 1 0 0 1 1 1 1 0 1 1 0 1 0 1 0 1 1 0 0 0 0 0 0 1 0 0 1
2	1 0 0 1 0 0 0 0 1 1 0 0 1 0 1 0 1 0 0 1 0 0 0 0 0 0 1 1 0 1 0 1
3	1 1 1 1 0 1 1 0 1 0 1 0 1 1 0 0 1 1 1 1 0 1 1 0 0 1 0 1 0 0 1 1
4	1 0 0 1 1 1 1 1 0 0 1 1 1 0 1 0 1 0 0 1 1 1 1 1 1 1 0 0 0 1 0 1
5	1 1 1 1 1 0 0 1 0 1 0 1 1 1 0 0 1 1 1 1 1 0 0 1 1 0 1 0 0 0 1 1
6	1 1 0 0 0 1 0 1 0 1 1 0 0 0 0 0 1 1 0 0 0 1 0 1 1 0 0 1 1 1 1 1
7	1 0 1 0 0 0 1 1 0 0 0 0 0 1 1 0 1 0 1 0 0 0 1 1 1 1 1 1 1 0 0 1
8	1 0 0 1 1 1 1 1 1 1 0 0 0 1 0 1 0 1 1 0 0 0 0 0 1 1 0 0 0 1 0 1
9	1 1 1 1 1 0 0 1 1 0 1 0 0 0 1 1 0 0 0 0 0 1 1 0 1 0 1 0 0 0 1 1
10	1 1 0 0 0 1 0 1 1 0 0 1 1 1 1 1 0 0 1 1 1 0 1 0 1 0 0 1 1 1 1 1
11	1 0 1 0 0 0 1 1 1 1 1 1 1 0 0 1 0 1 0 1 1 1 0 0 1 1 1 1 1 0 0 1
12	1 1 0 0 1 0 1 0 0 1 1 0 1 1 1 1 0 0 1 1 0 1 0 1 0 1 1 0 1 1 1 1
13	1 0 1 0 1 1 0 0 0 0 0 0 1 0 0 1 0 1 0 1 0 0 1 1 0 0 0 0 1 0 0 1
14	1 0 0 1 0 0 0 0 0 0 1 1 0 1 0 1 0 1 1 0 1 1 1 1 0 0 1 1 0 1 0 1
15	1 1 1 1 0 1 1 0 0 1 0 1 0 0 1 1 0 0 0 0 1 0 0 1 0 1 0 1 0 0 1 1

25. The apparatus according to claim 23 or 24, wherein at least two columns of elements in a matrix formed by the chip sequence are the same.

26. A communication apparatus, comprising a processor and a memory, wherein

the memory is configured to store instructions; and

the processor is configured to execute the instructions, so that the method according to any one of claims 1 to 16 is implemented.

27. A chip, comprising a logic circuit and an interface, wherein the logic circuit is coupled to the interface; and

the interface is configured to input and/or output code instructions, and the logic circuit is configured to execute the code instructions, so that the method according to any one of claims 1 to 16 is implemented.

28. A computer-readable storage medium, wherein the computer-readable storage medium is configured to store a computer program, and when the computer program is executed, the method according to any one of claims 1 to 16 is performed.

29. A communication system, wherein the communication system comprises a transmit end and a receive end, the transmit end is configured to perform the method according to any one of claims 1 and 4 to 16, and the receive end is configured to perform the method according to any one of claims 2 to 16.