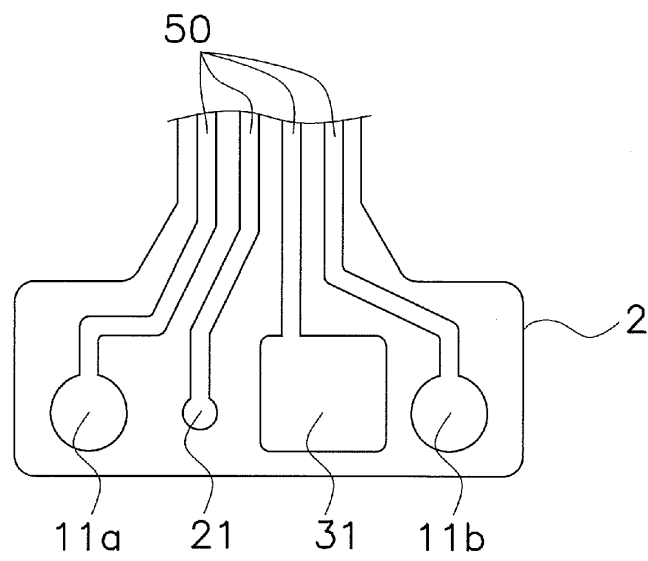
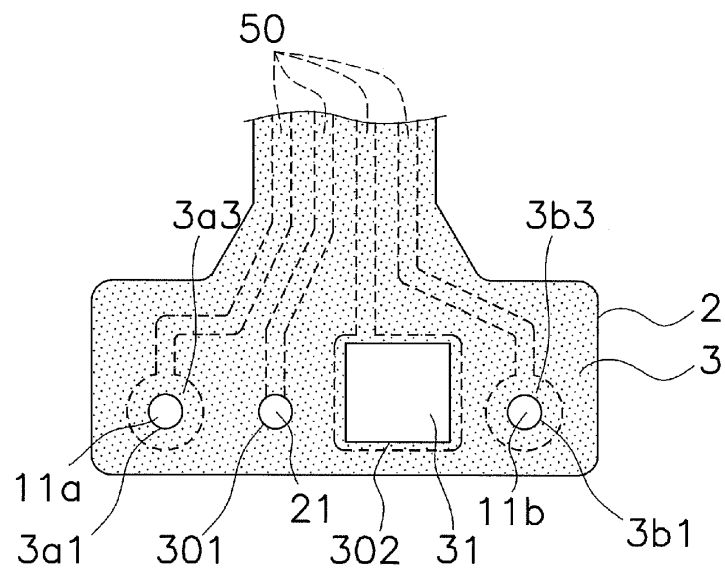


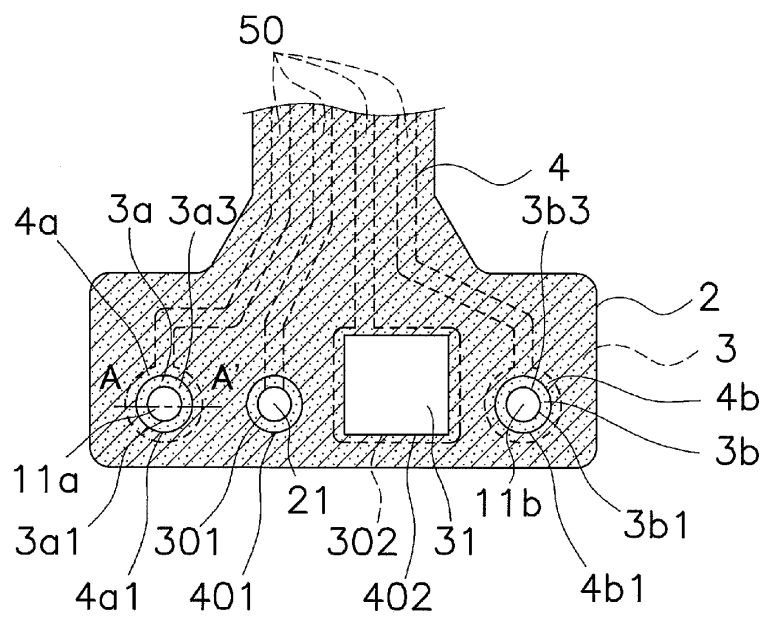
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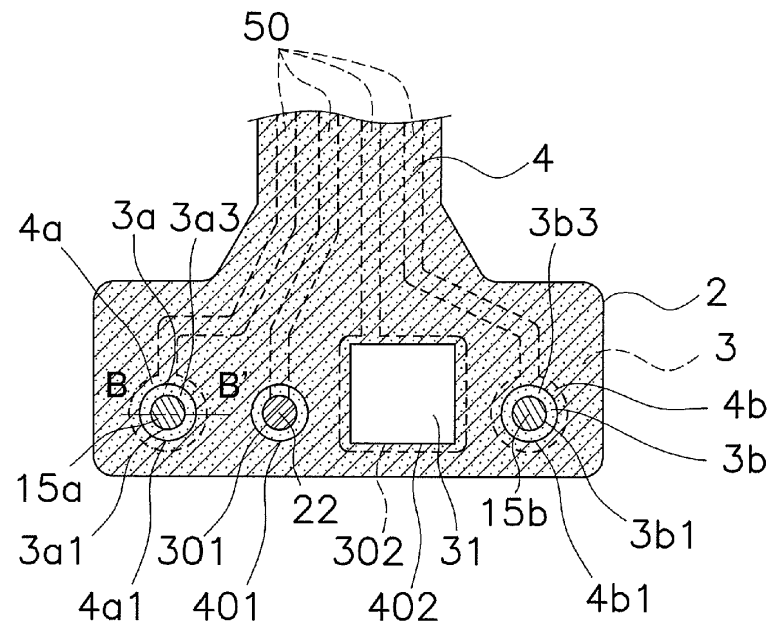
[図2]



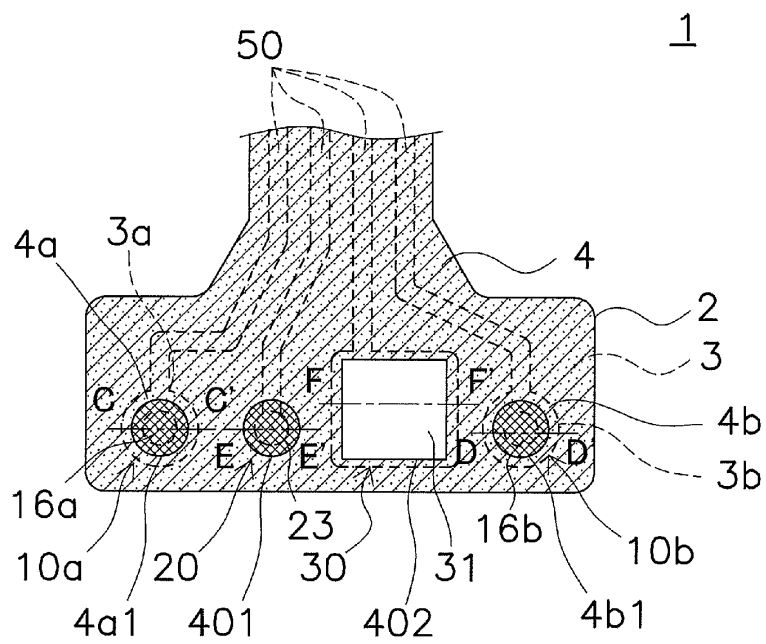
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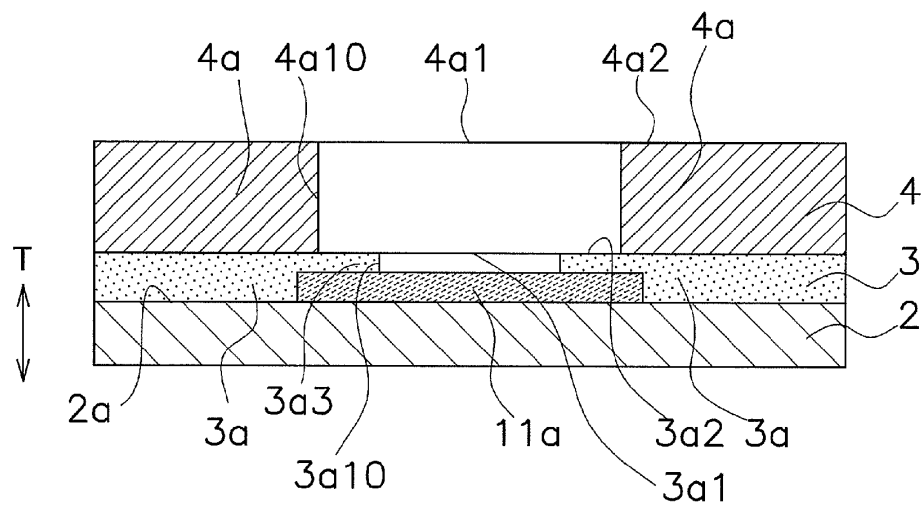
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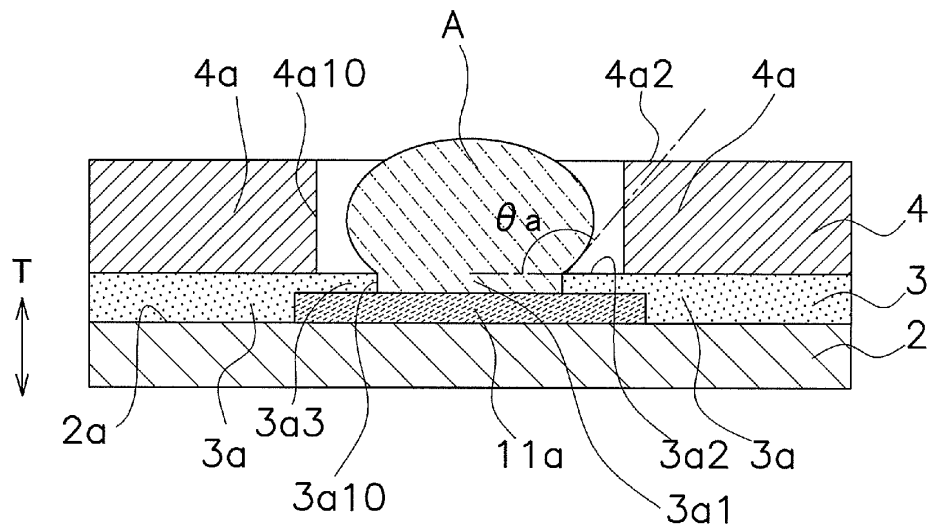
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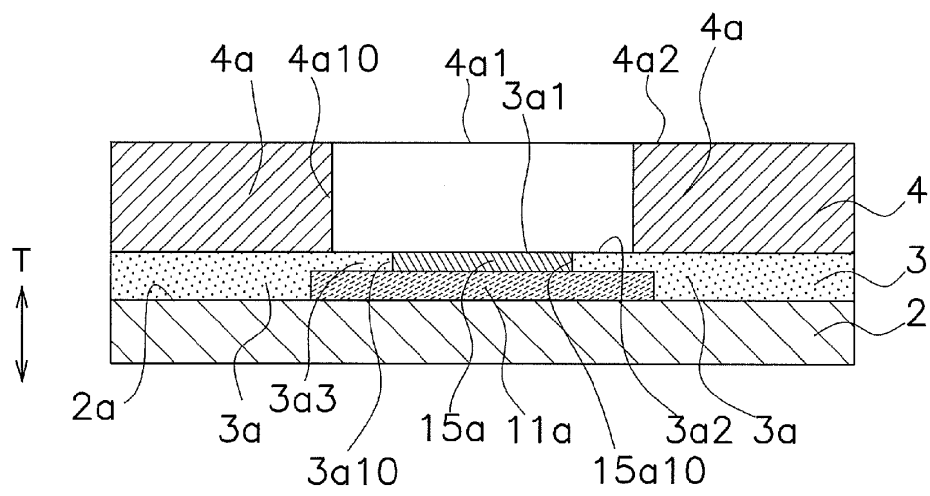
[図6]



[図7]



[図8]



[図9]

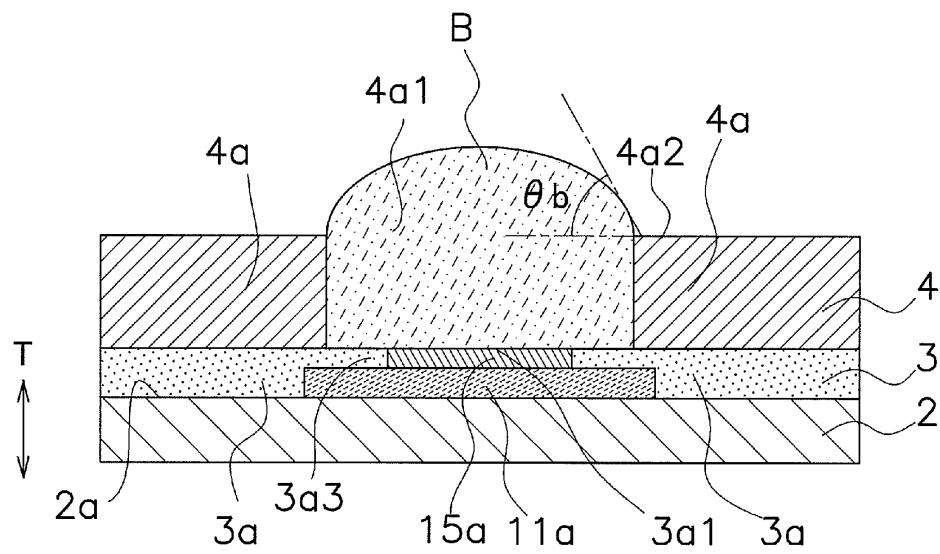
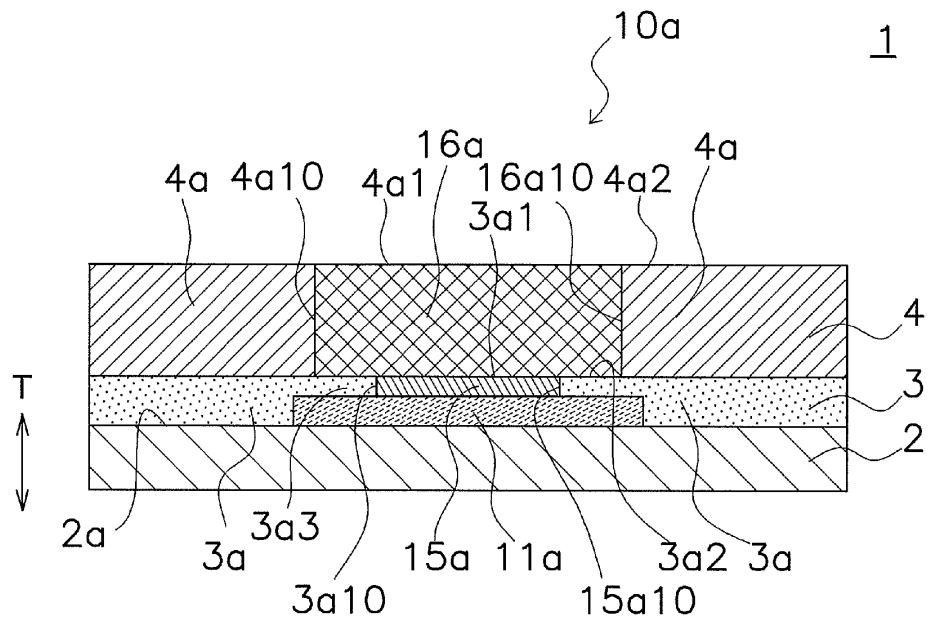


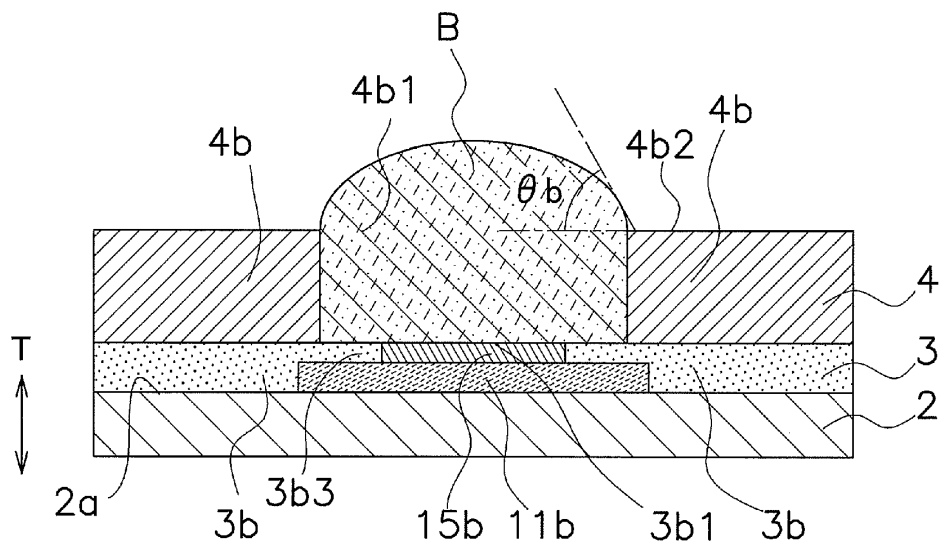
Fig. 1 is a cross-sectional view of a semiconductor device. The device consists of a substrate 2. On top of the substrate 2, there is a layer 3. Layer 3 is divided into a central region 3a3 (cross-hatched) and side regions 3a1 (dotted) and 3a (hatched). A layer 4 is on top of layer 3. Layer 4 is divided into a central region 4a1 (white) and side regions 4a (hatched). A vertical dimension T is indicated on the left.

Diagram illustrating a cross-sectional view of a semiconductor device. The structure includes a substrate (2) with a central region (11a) containing a structure (15a). A dome-shaped region (16a) is formed on top of 11a, surrounded by a ring (4a). A vertical arrow T indicates a direction.

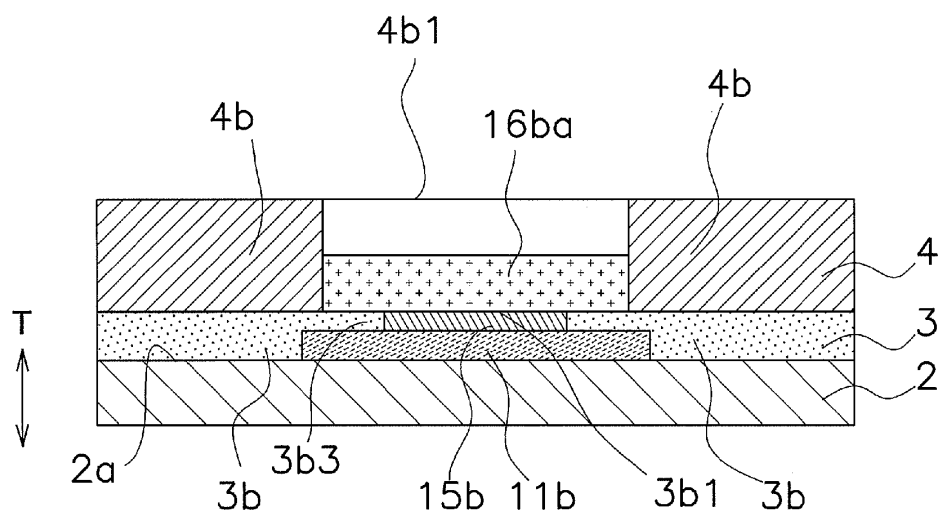
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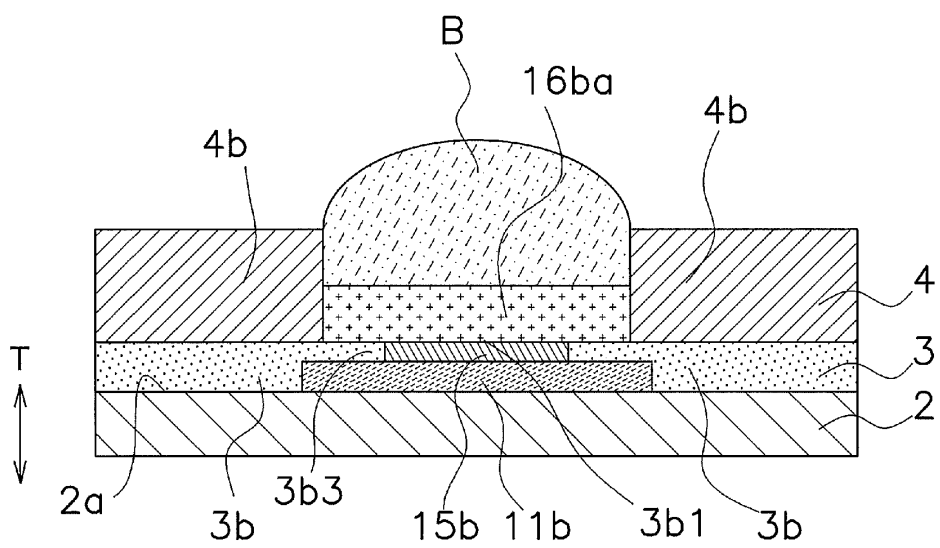
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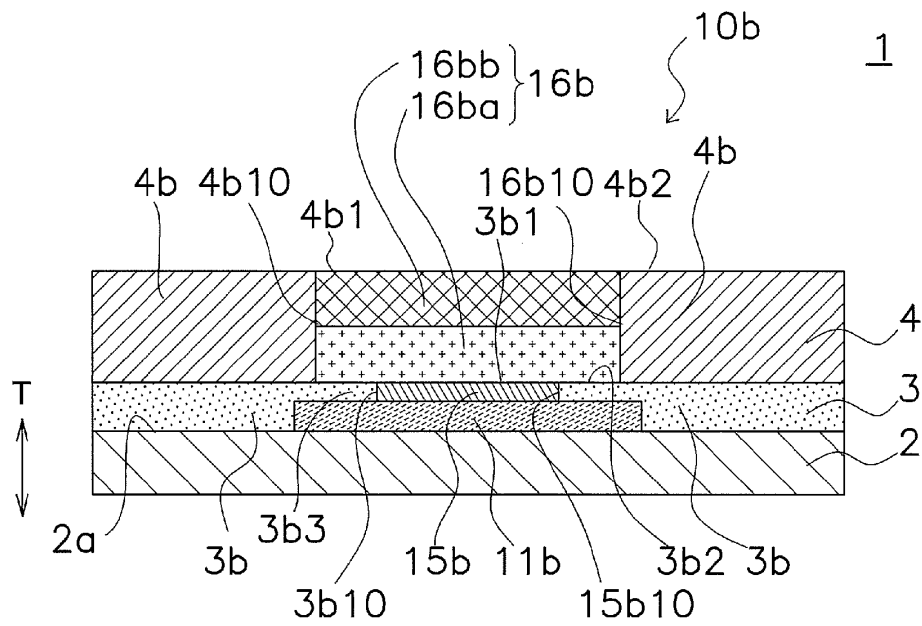
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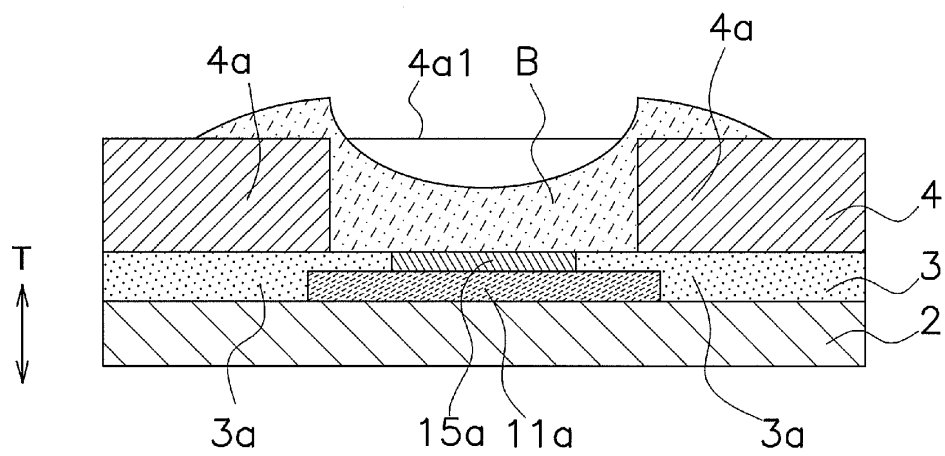
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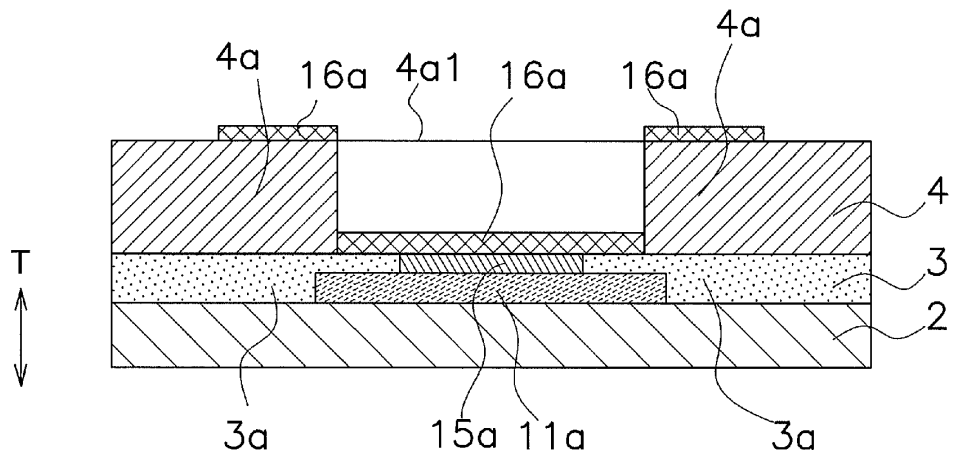
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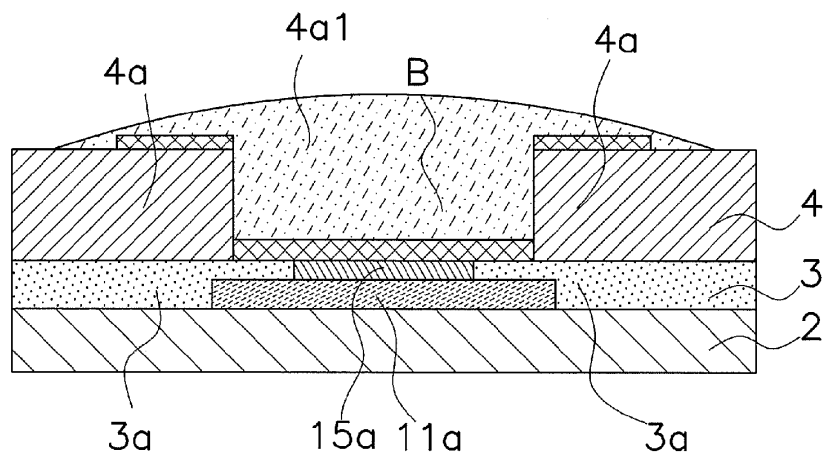
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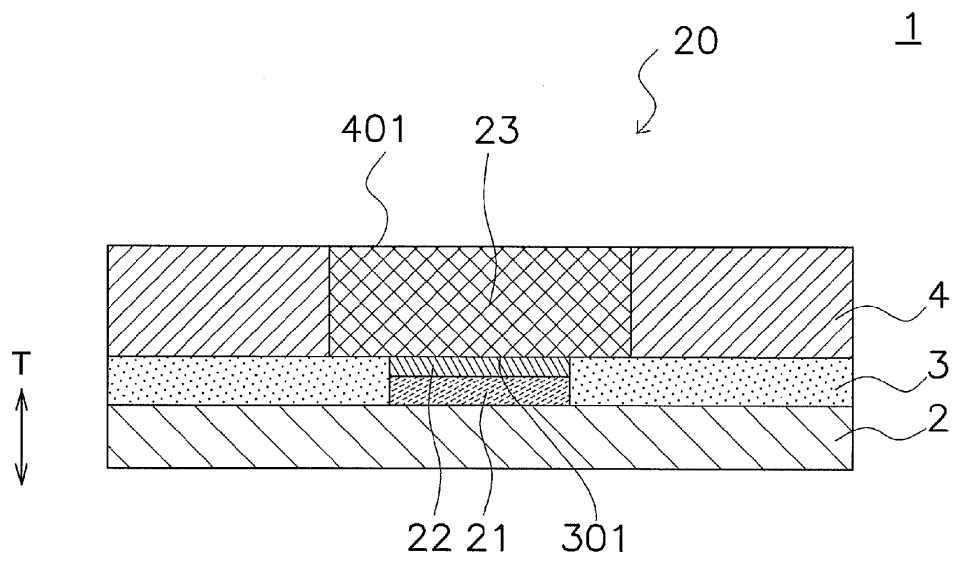
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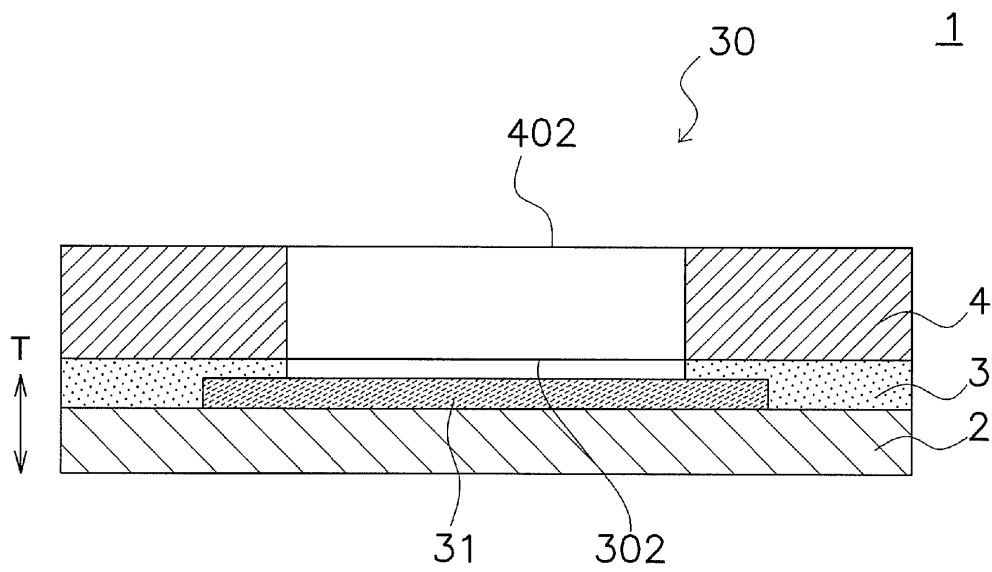
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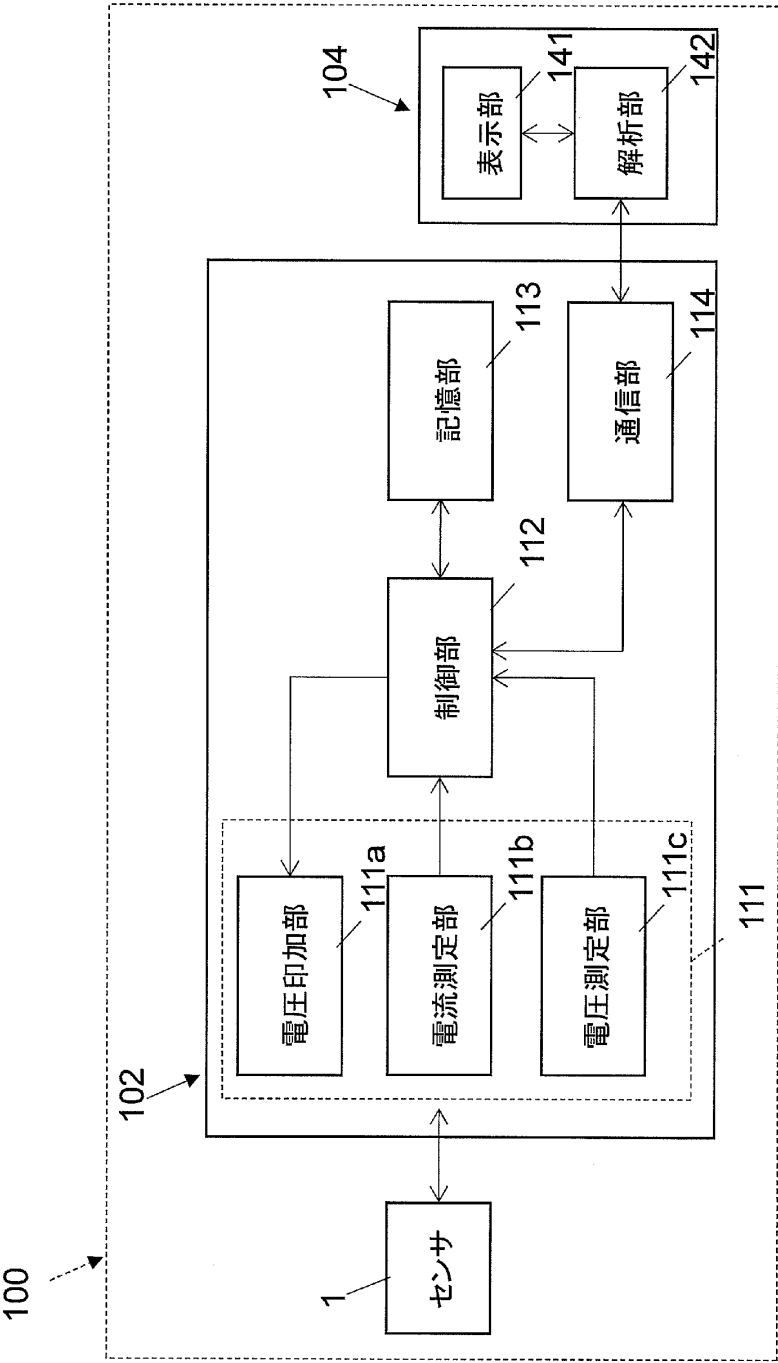
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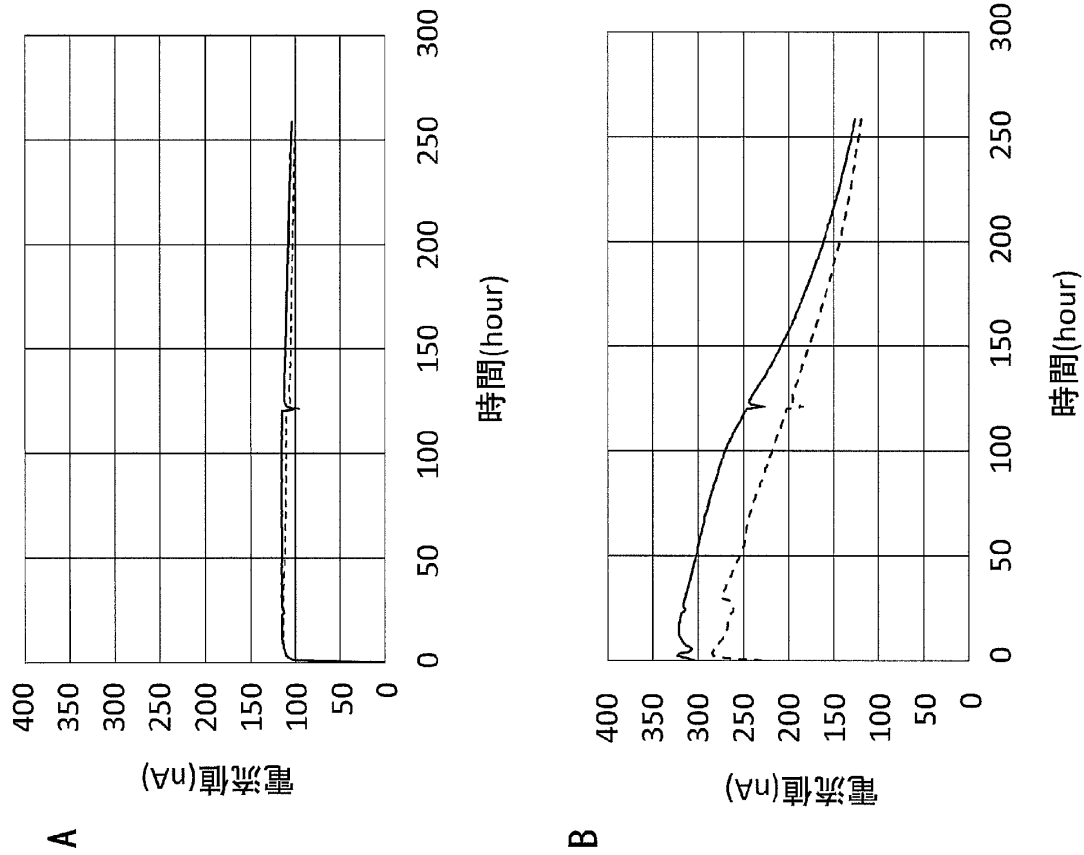
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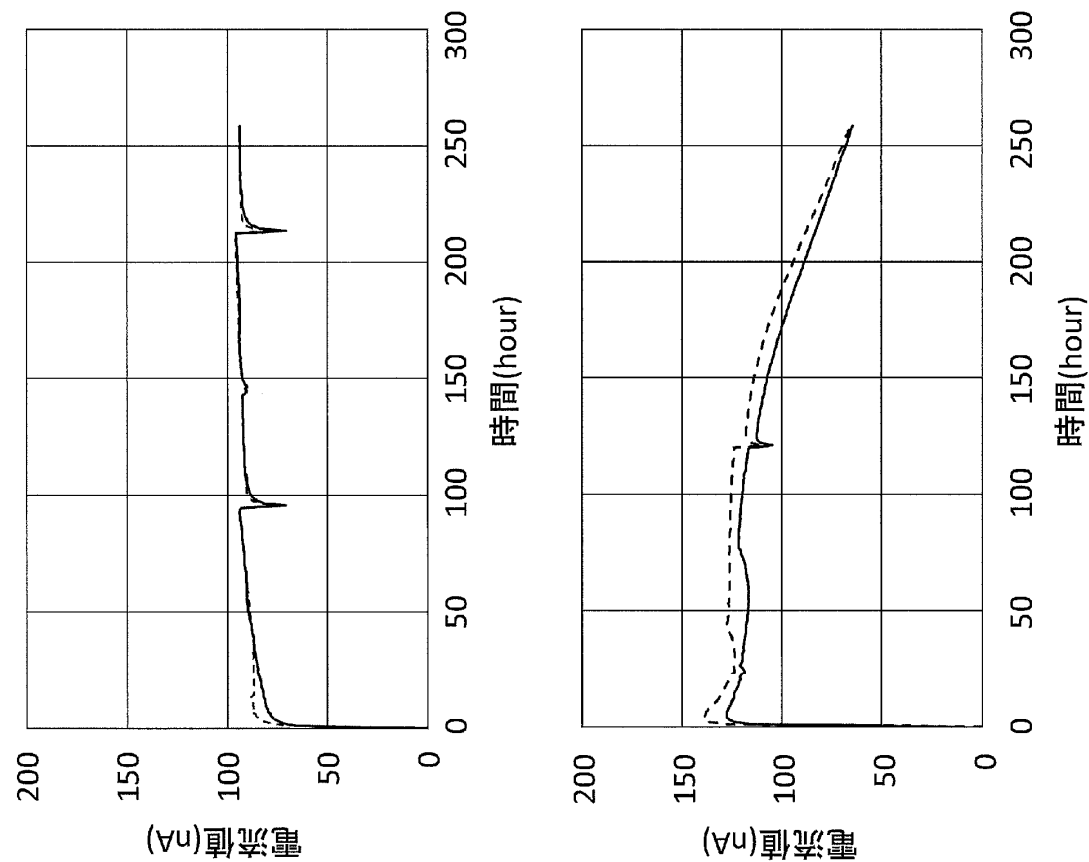
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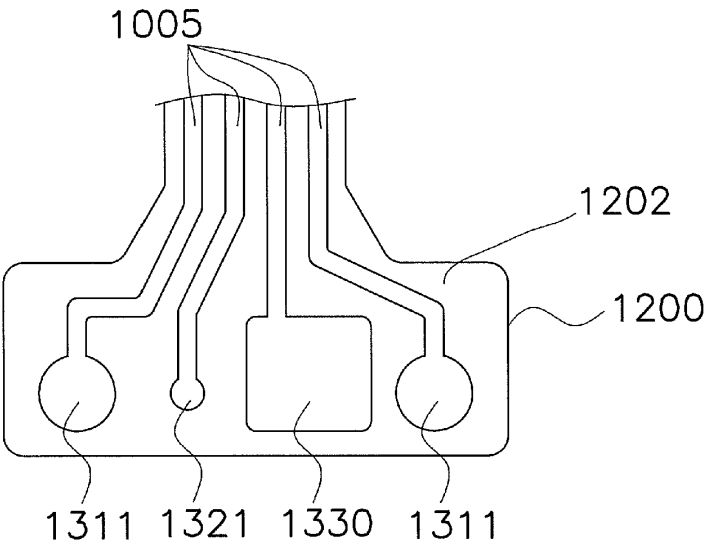
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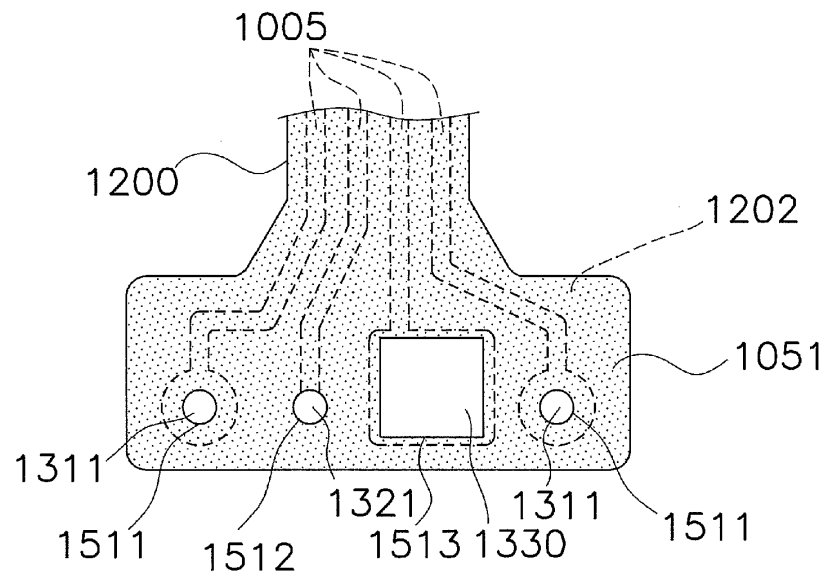
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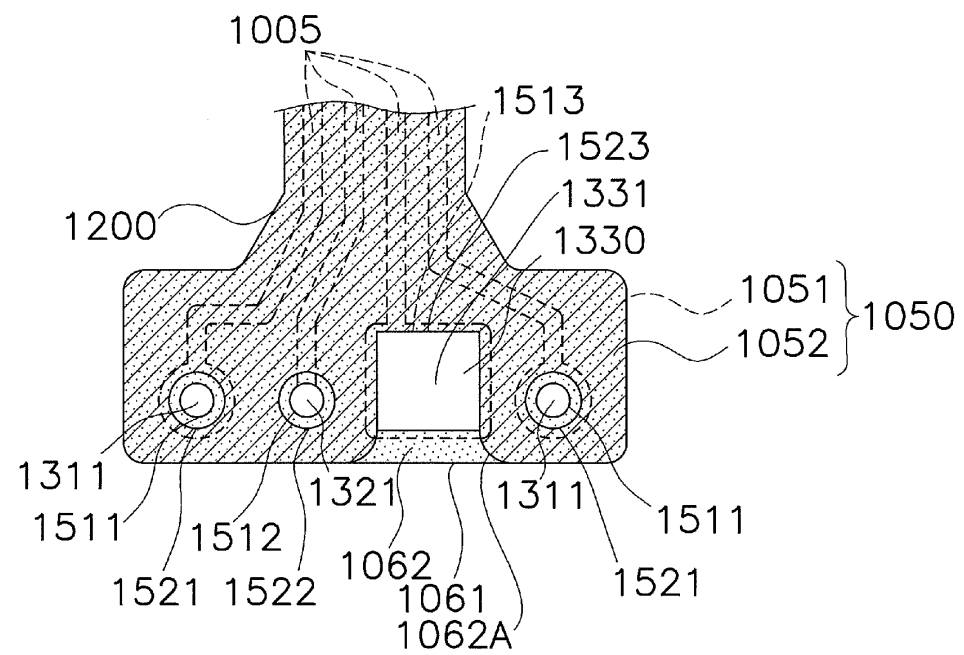
A
[図27]



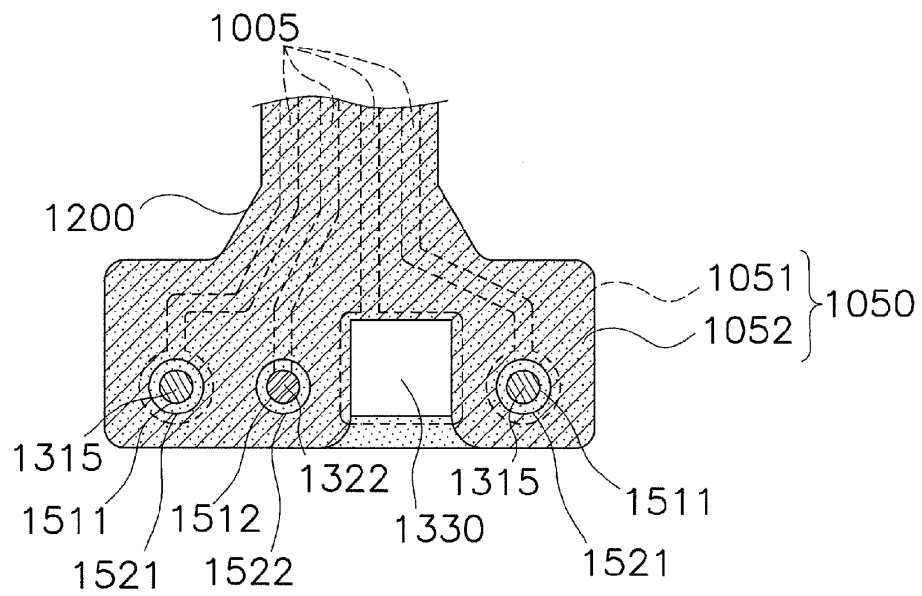
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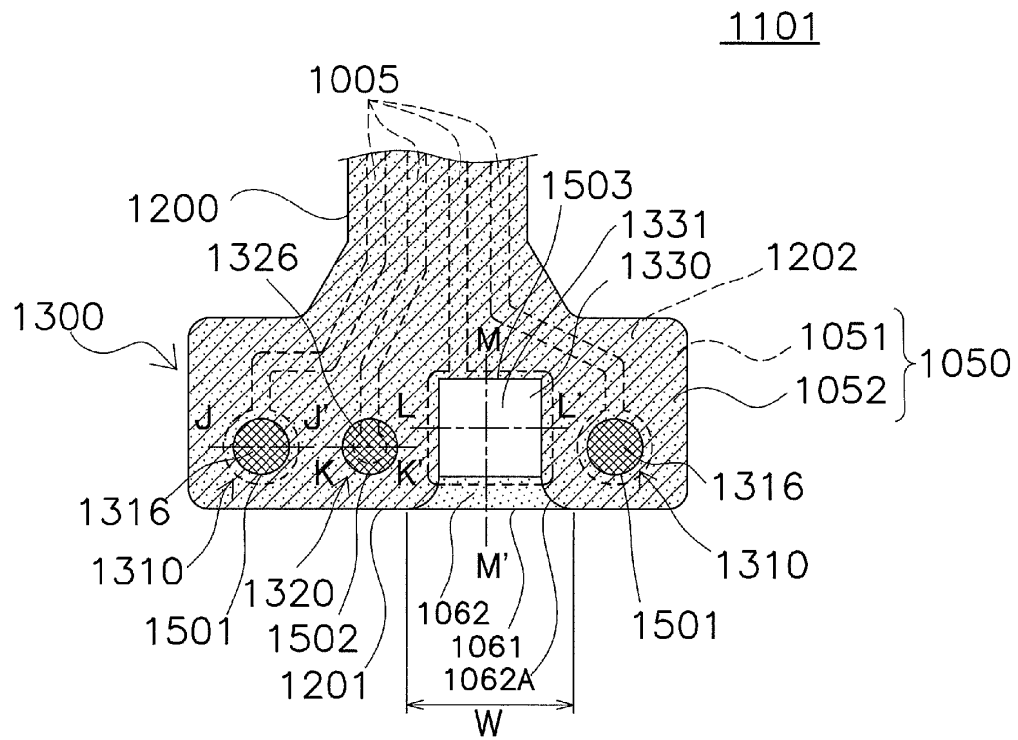
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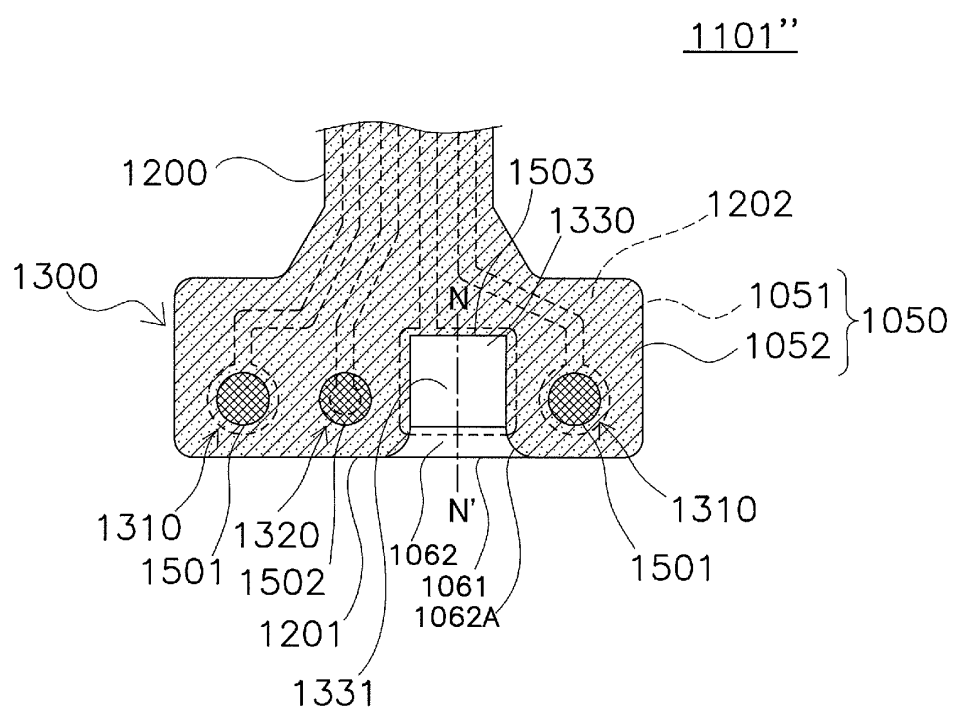
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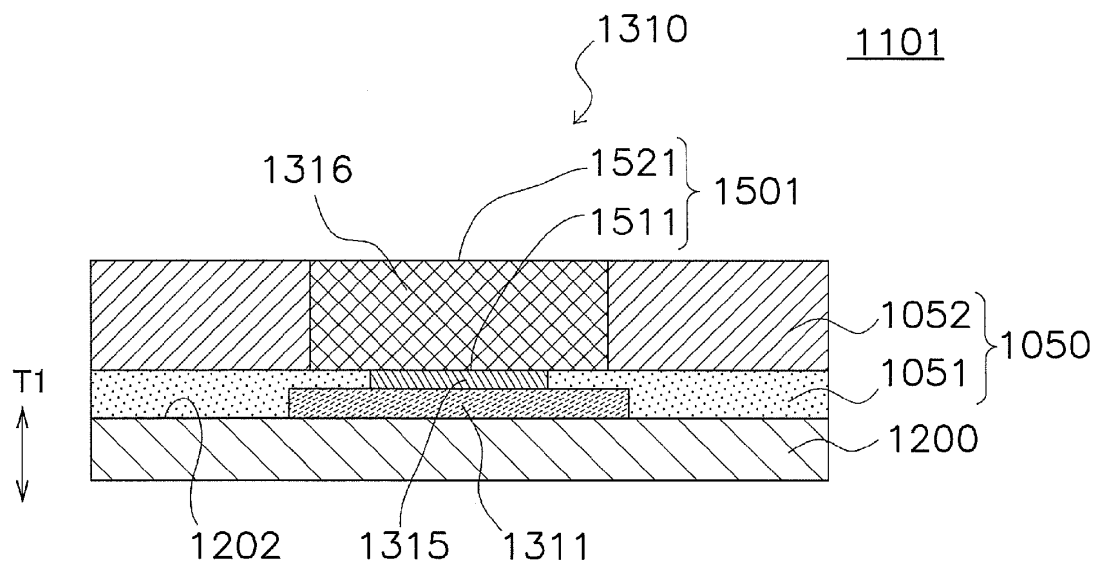
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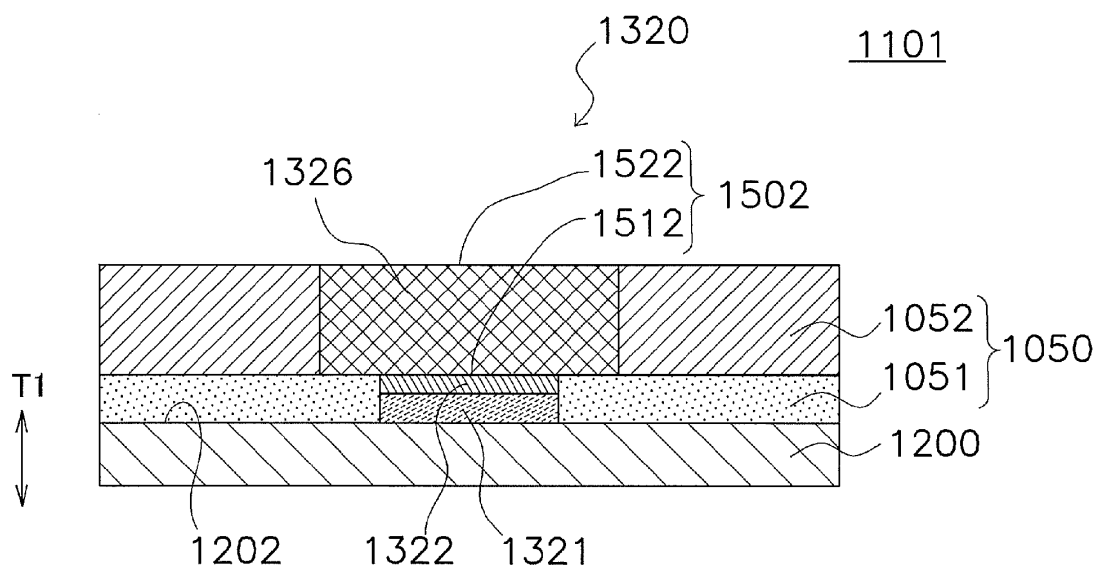
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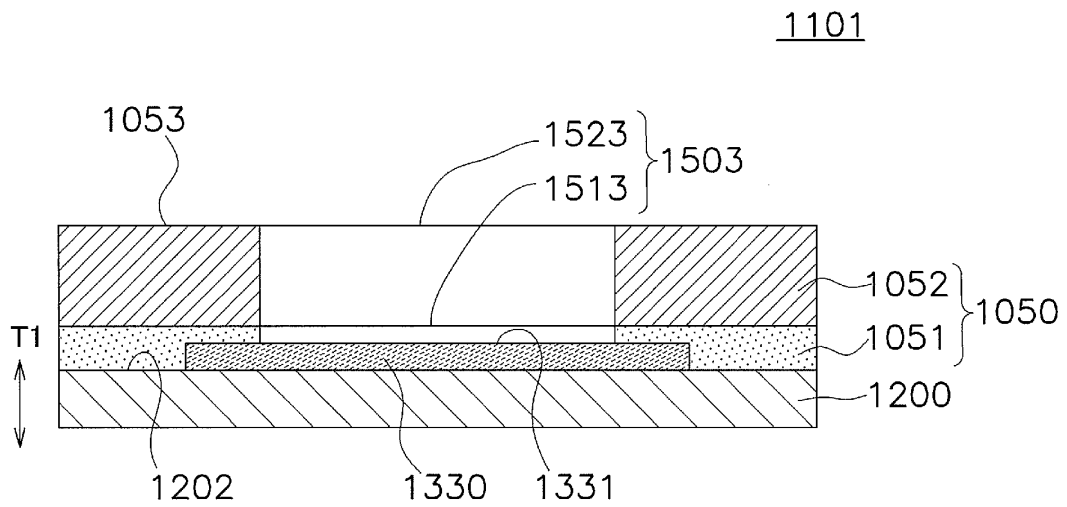
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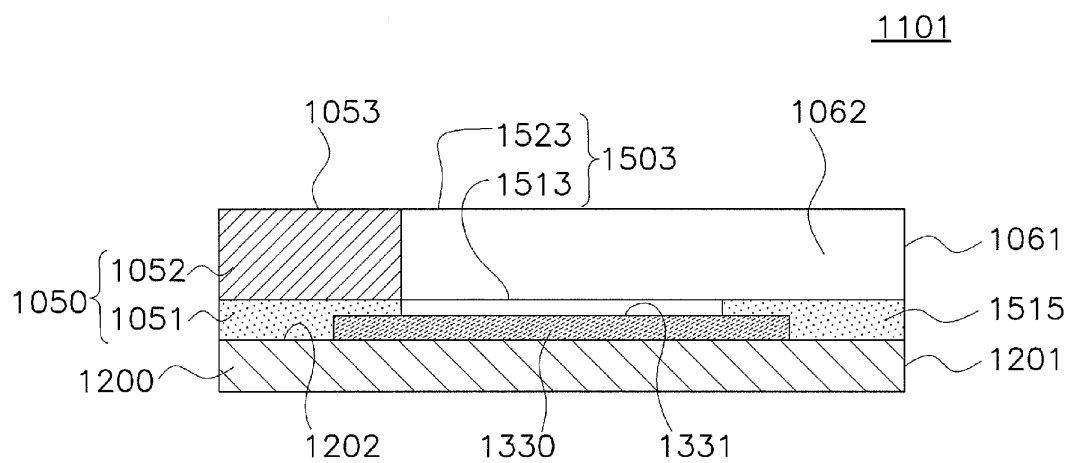
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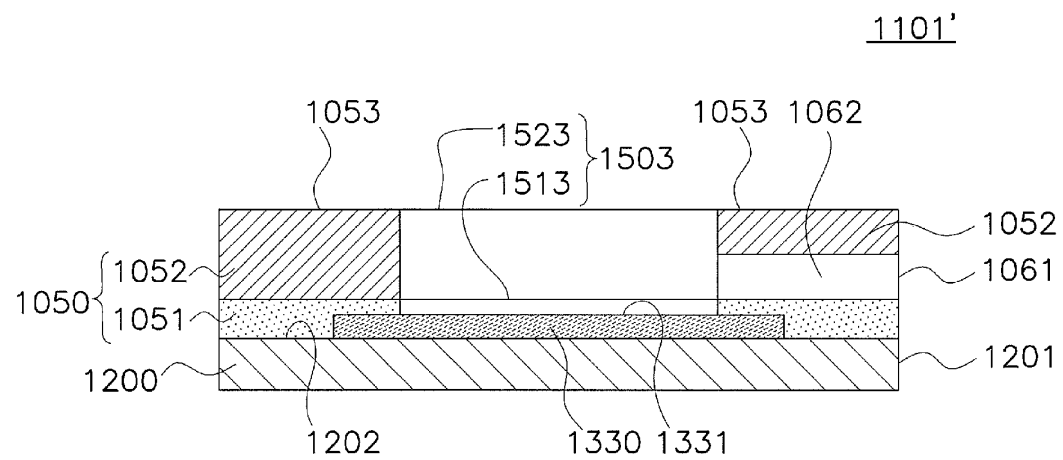
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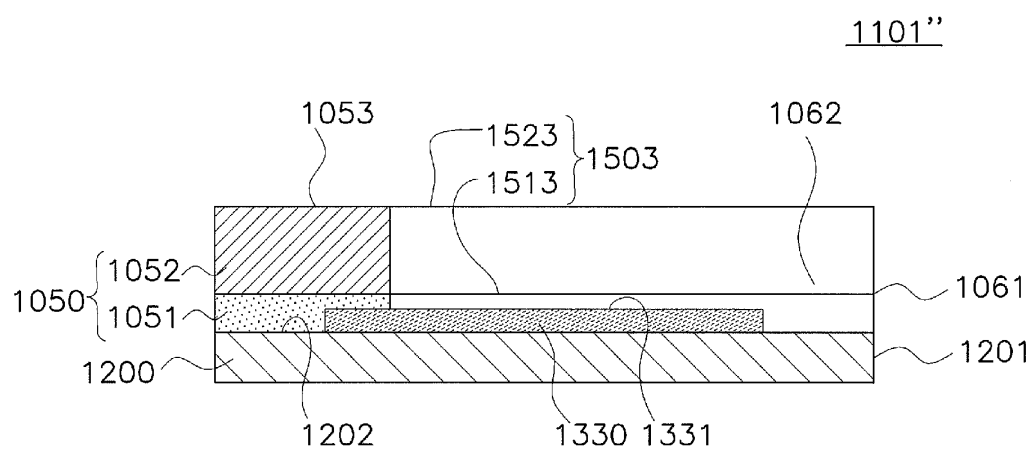
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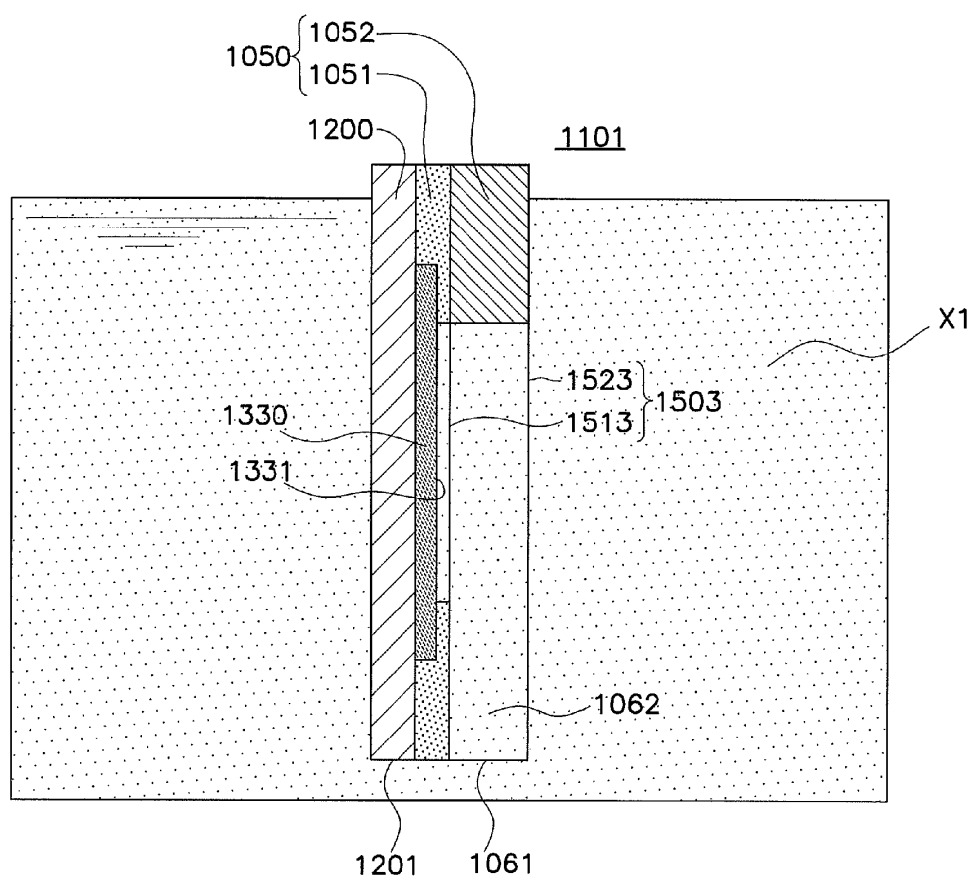
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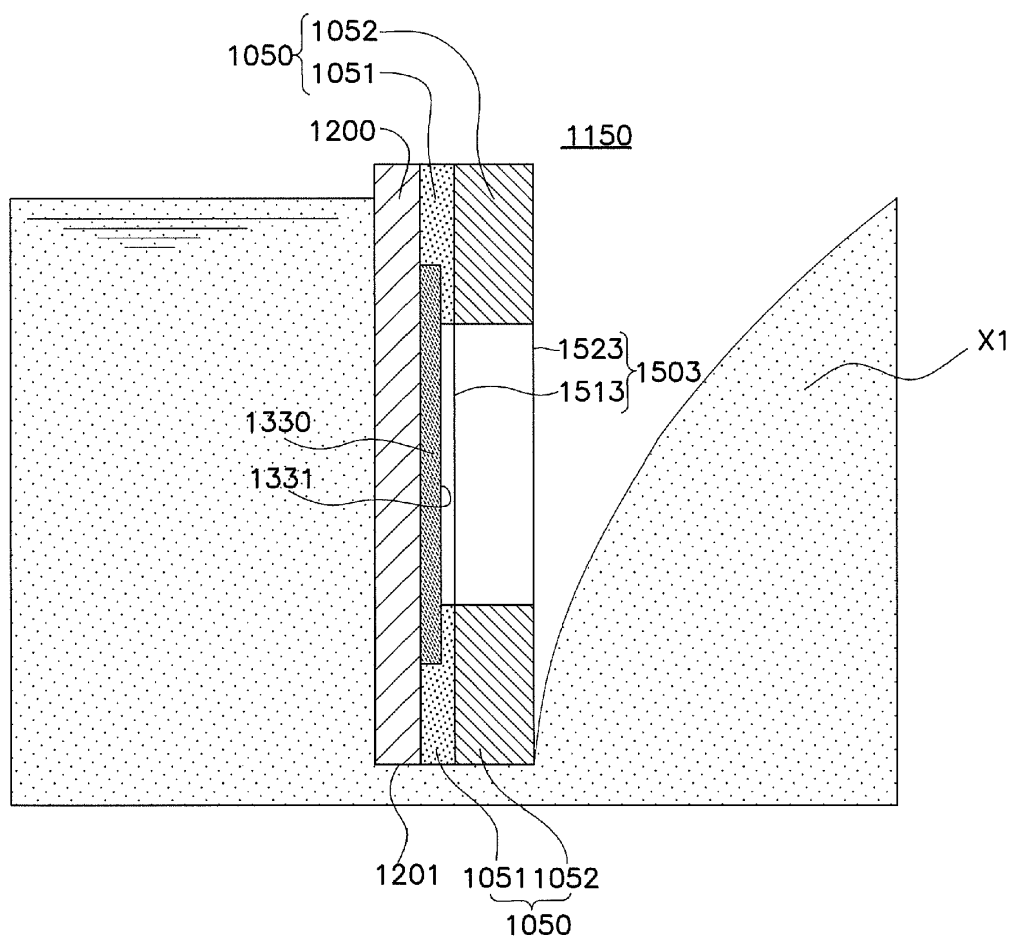
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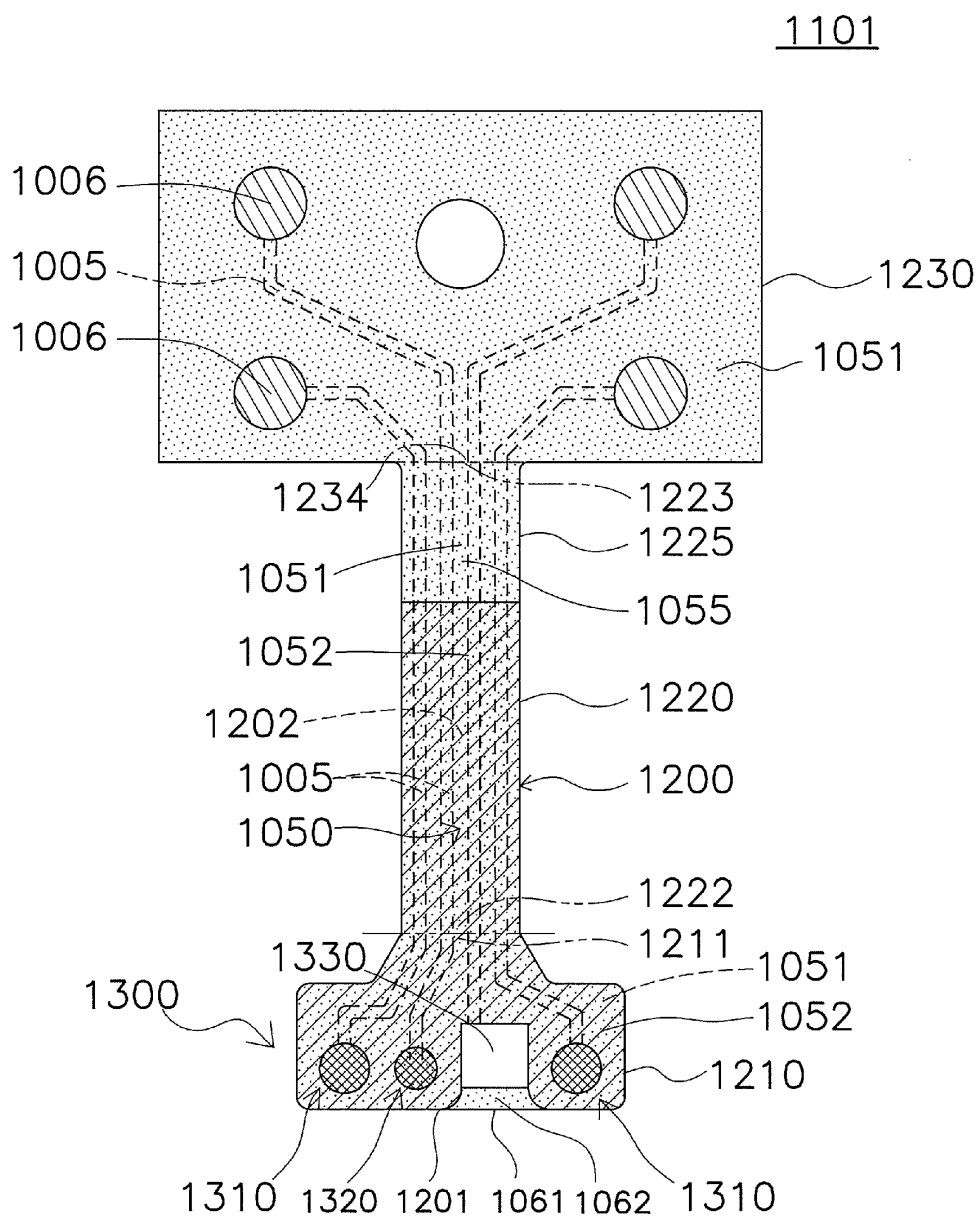
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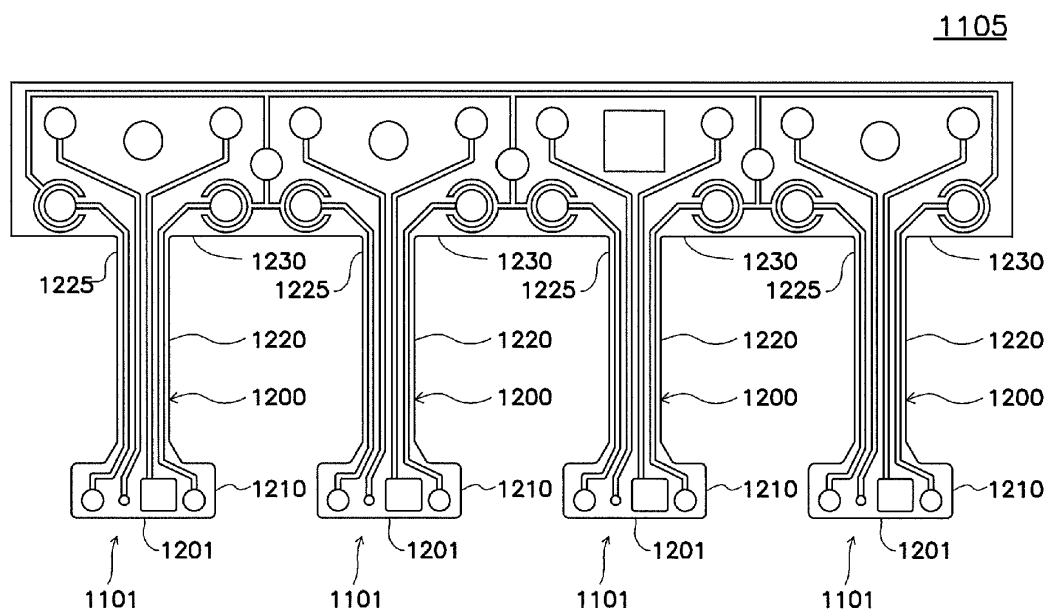
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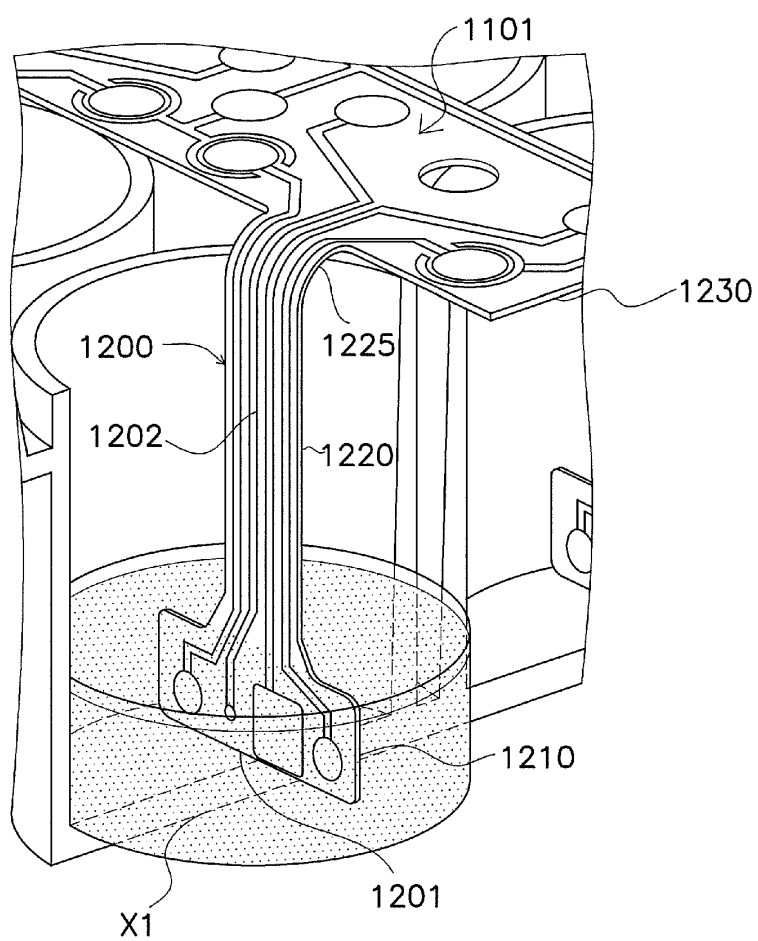
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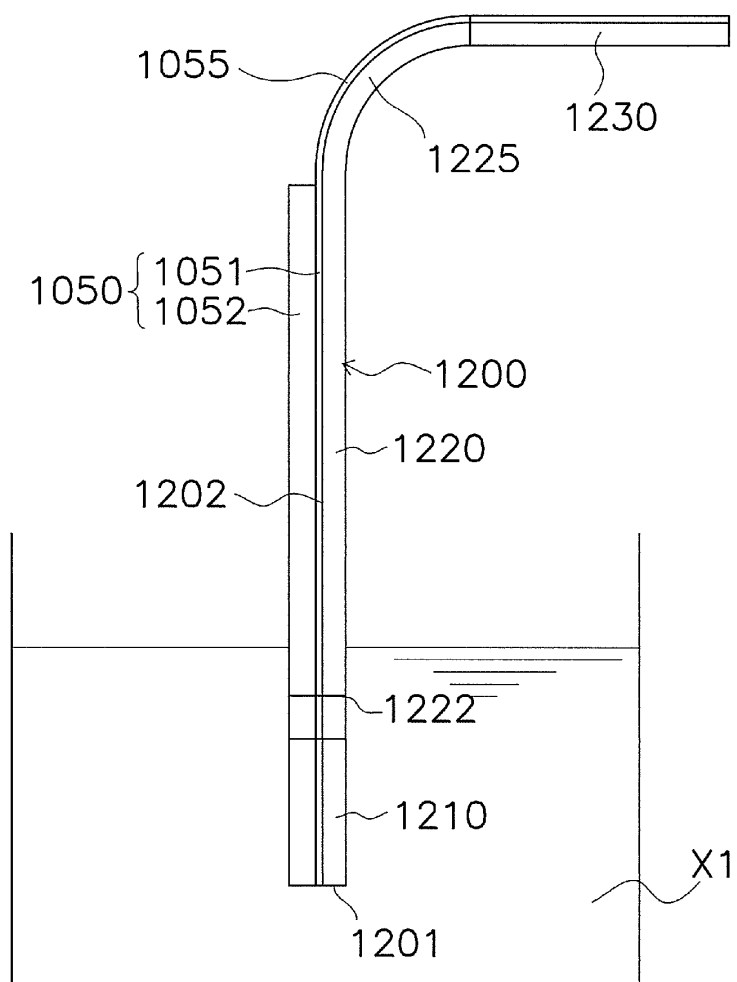
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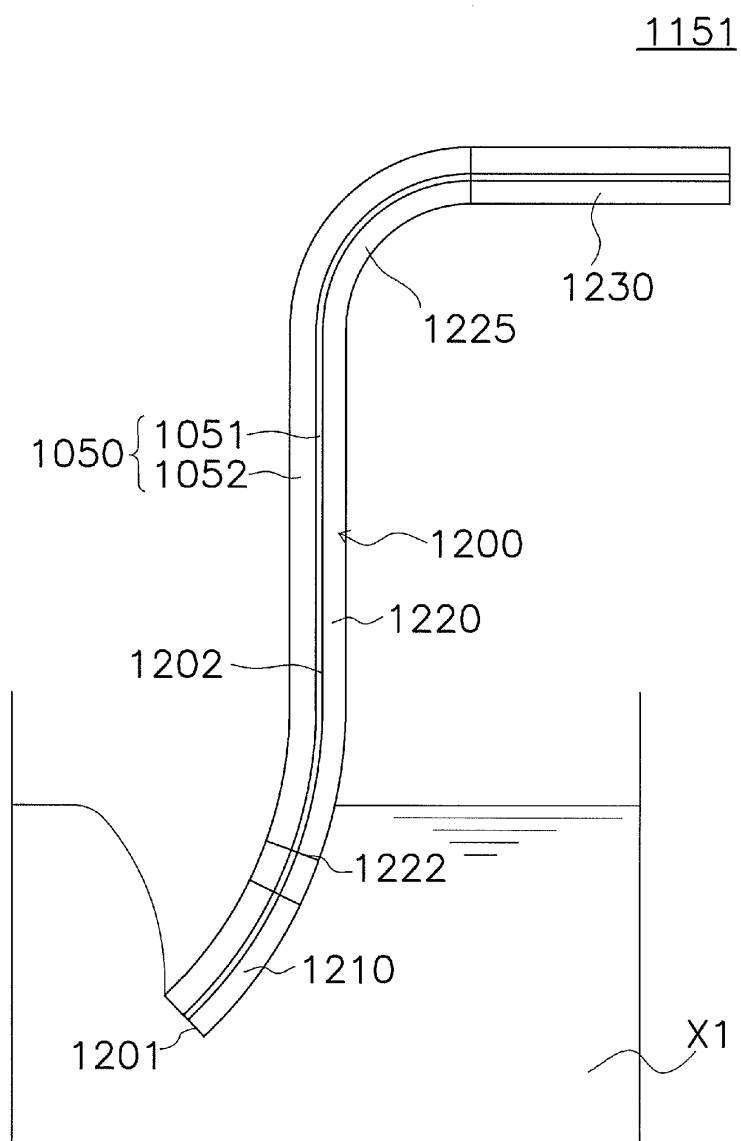
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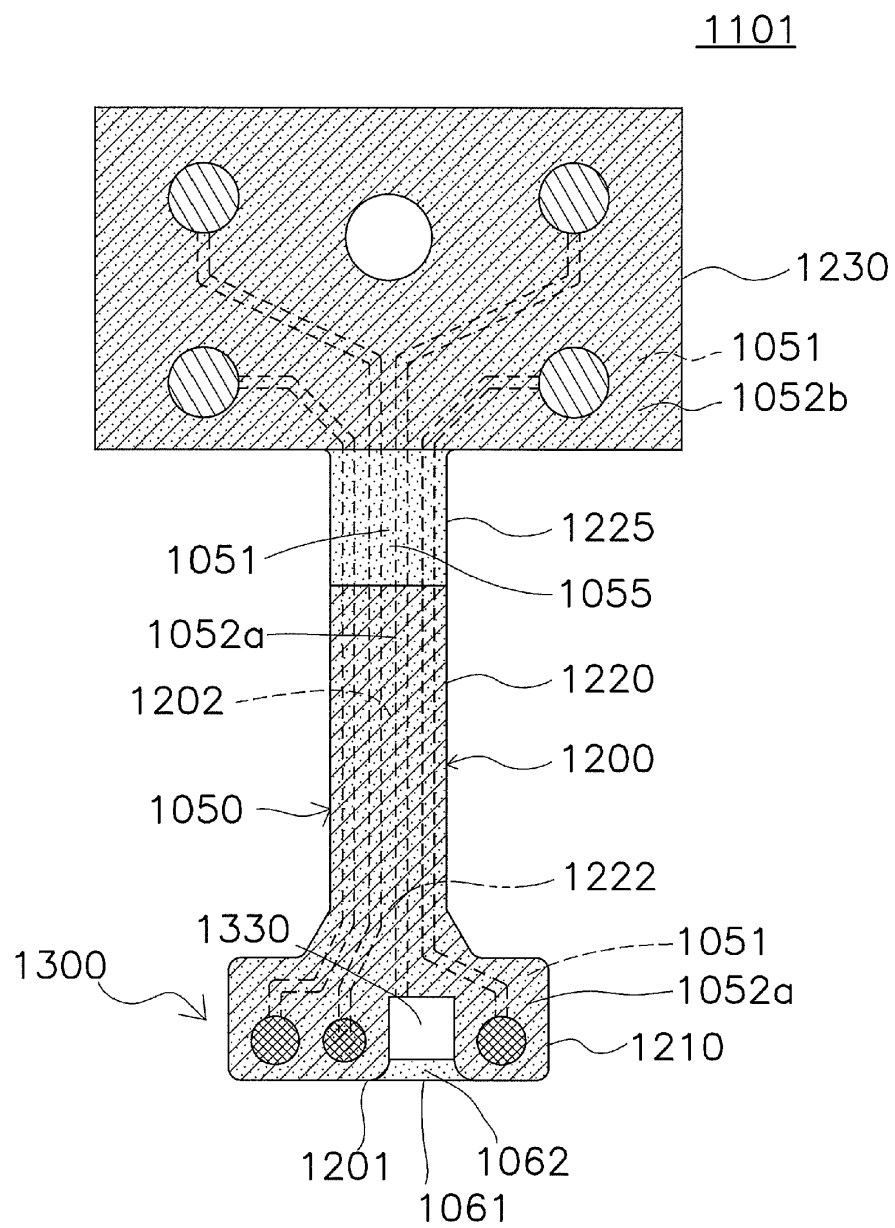
[図44]

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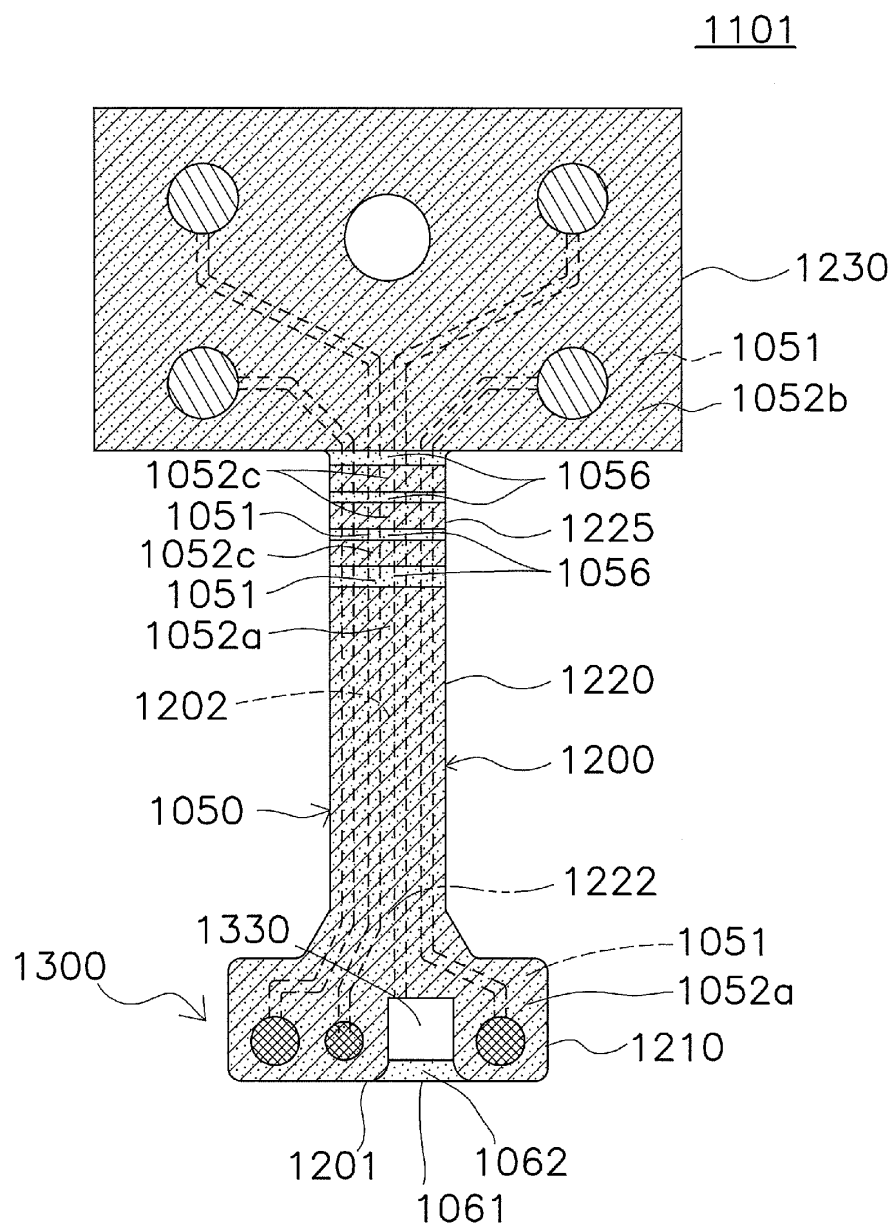
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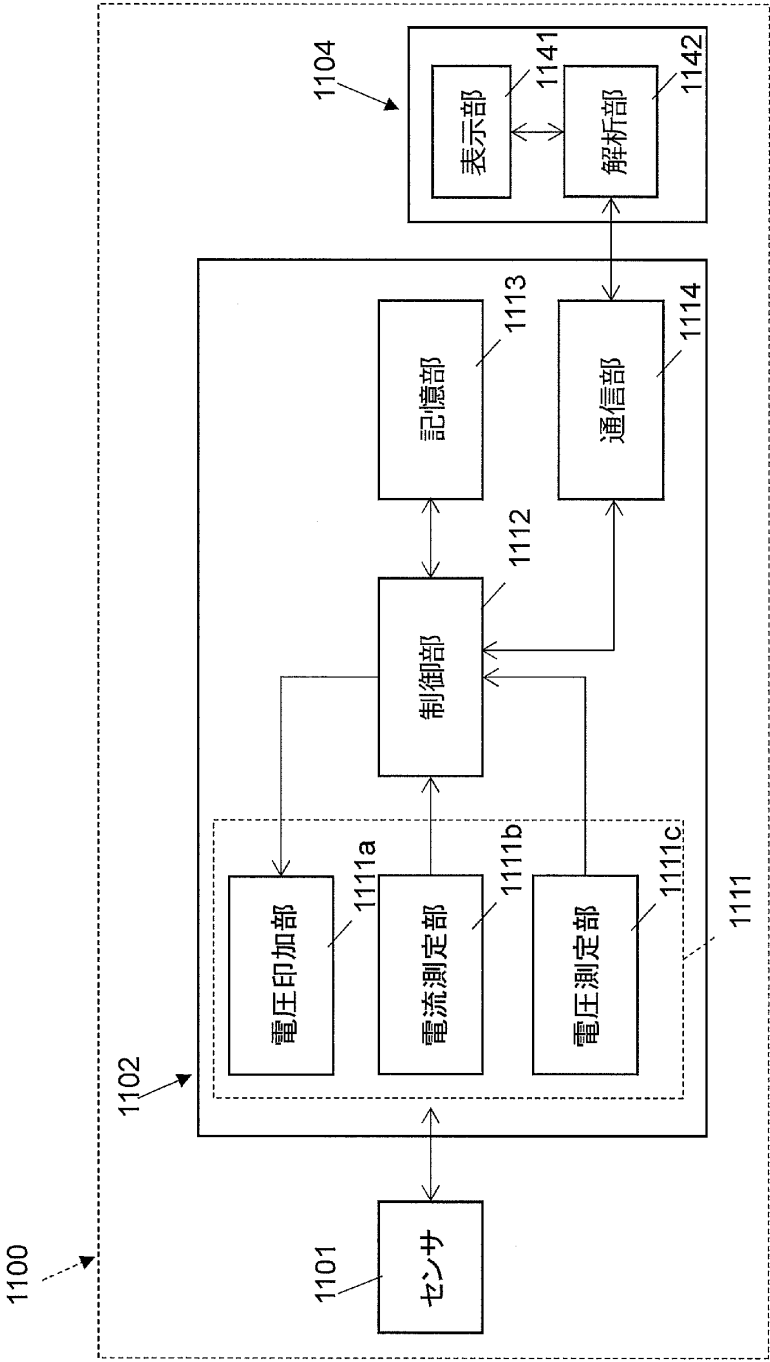
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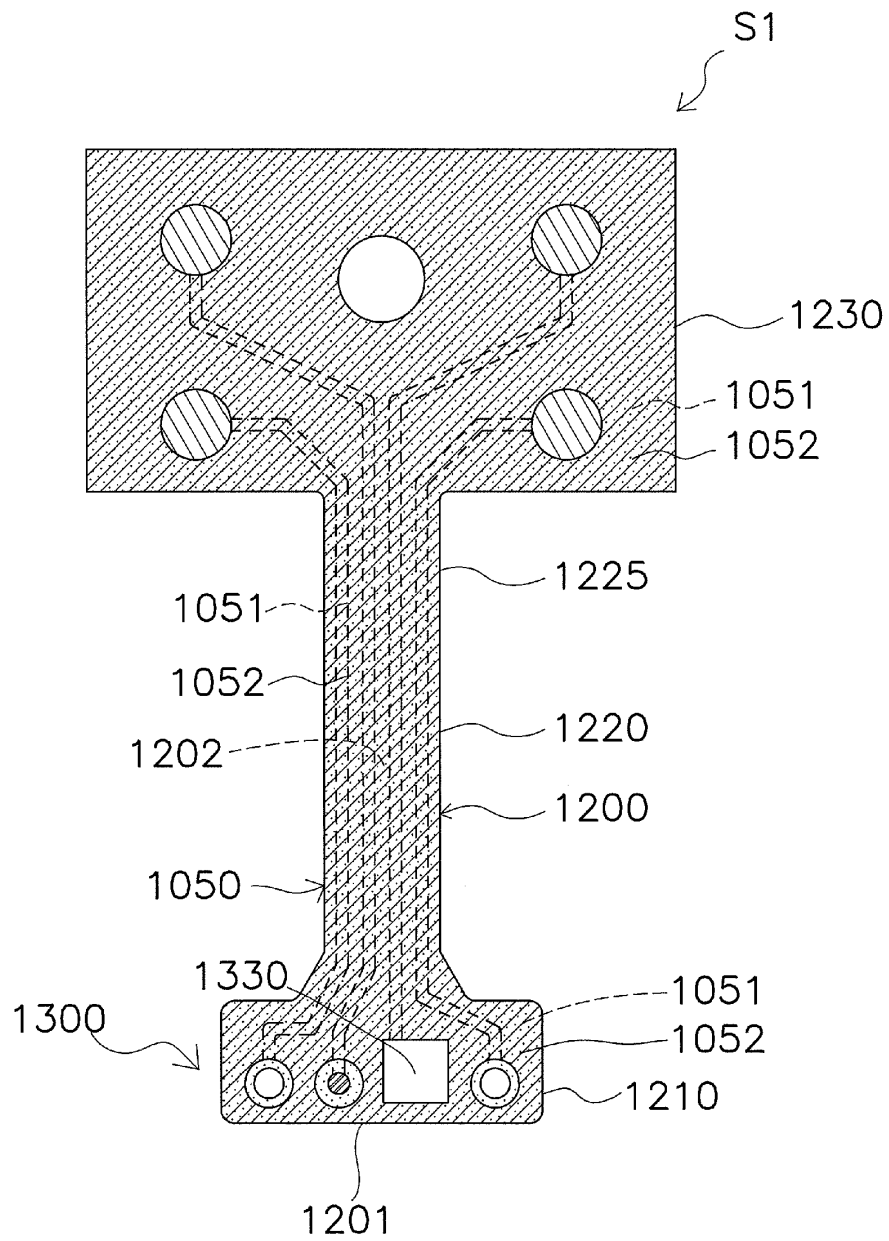
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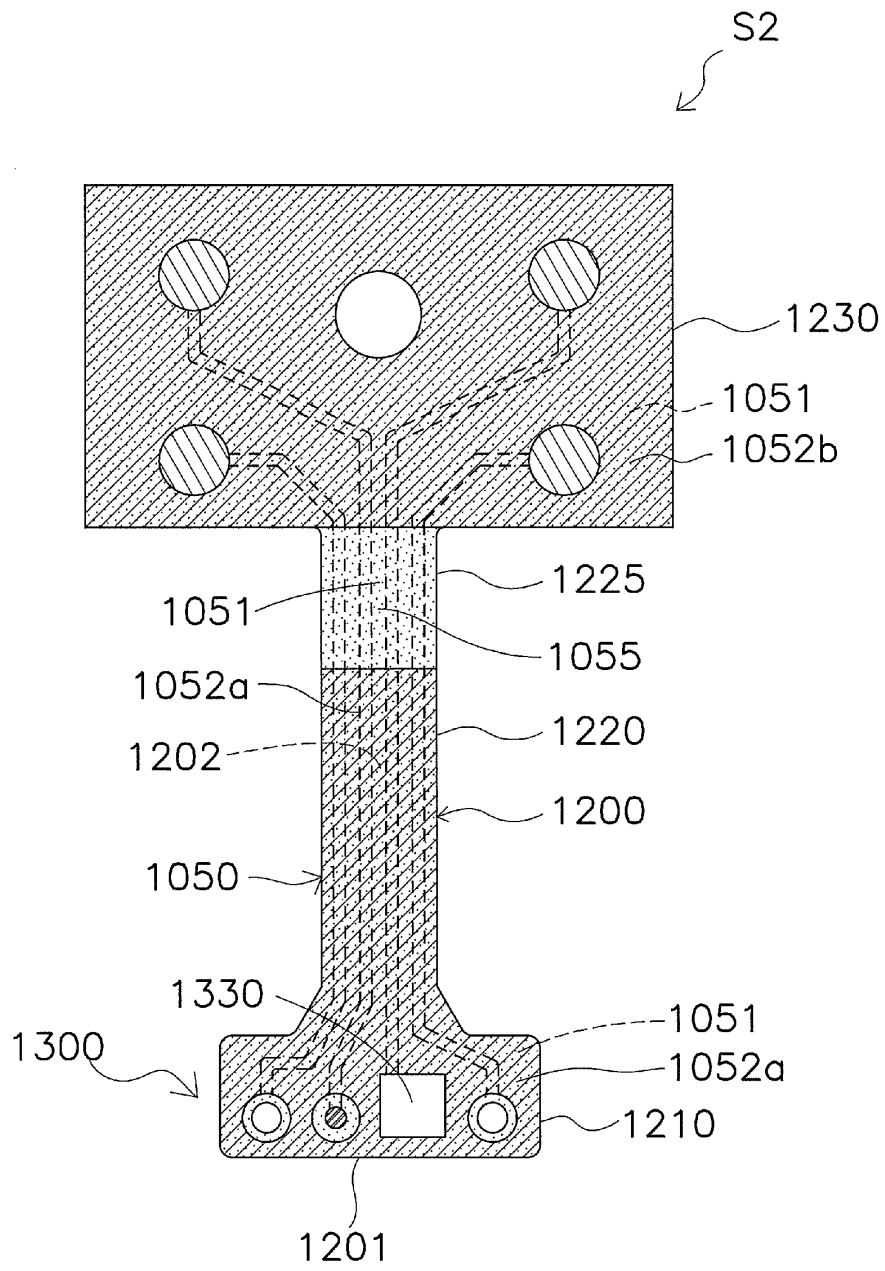
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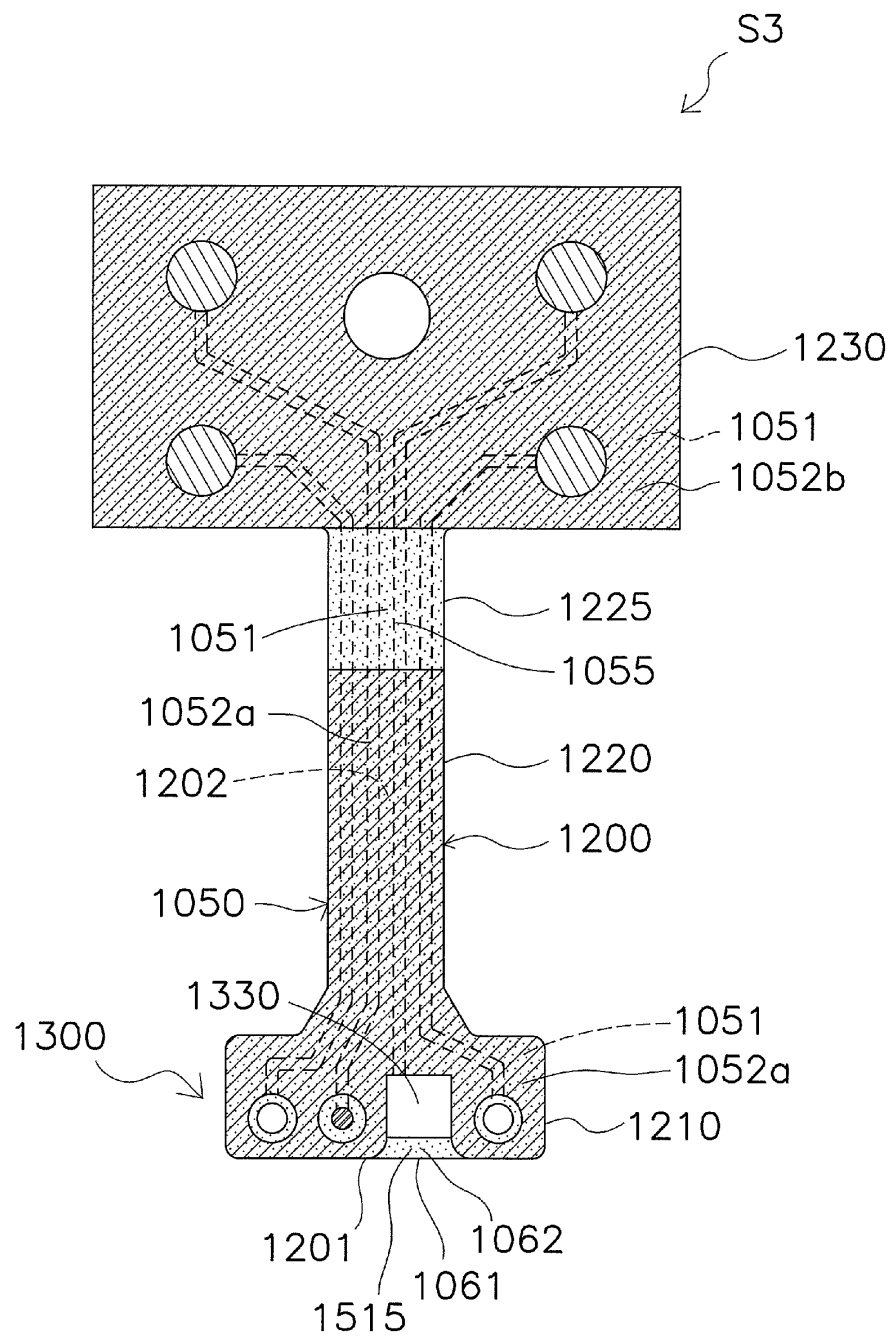
[図49A]



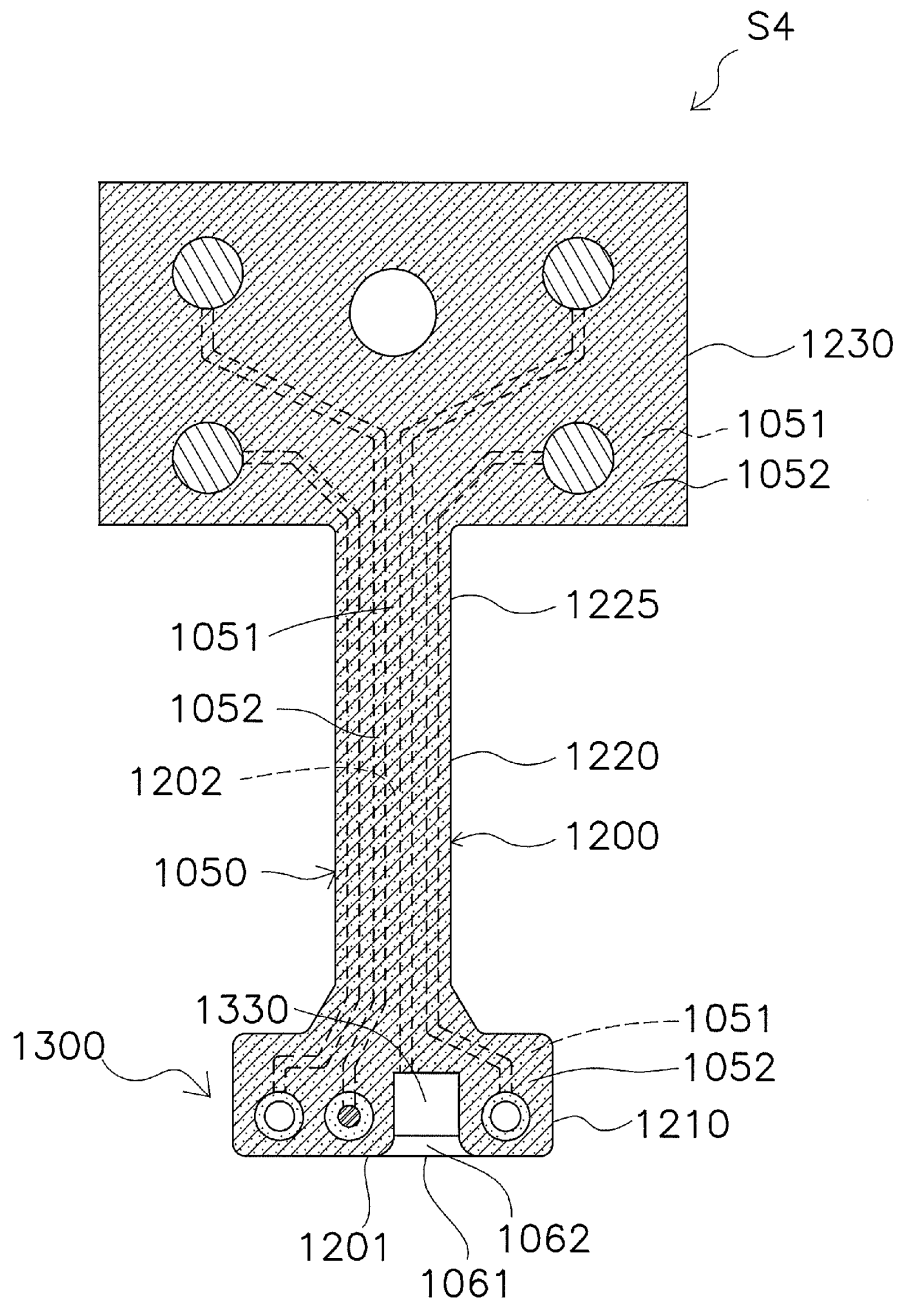
[図49B]



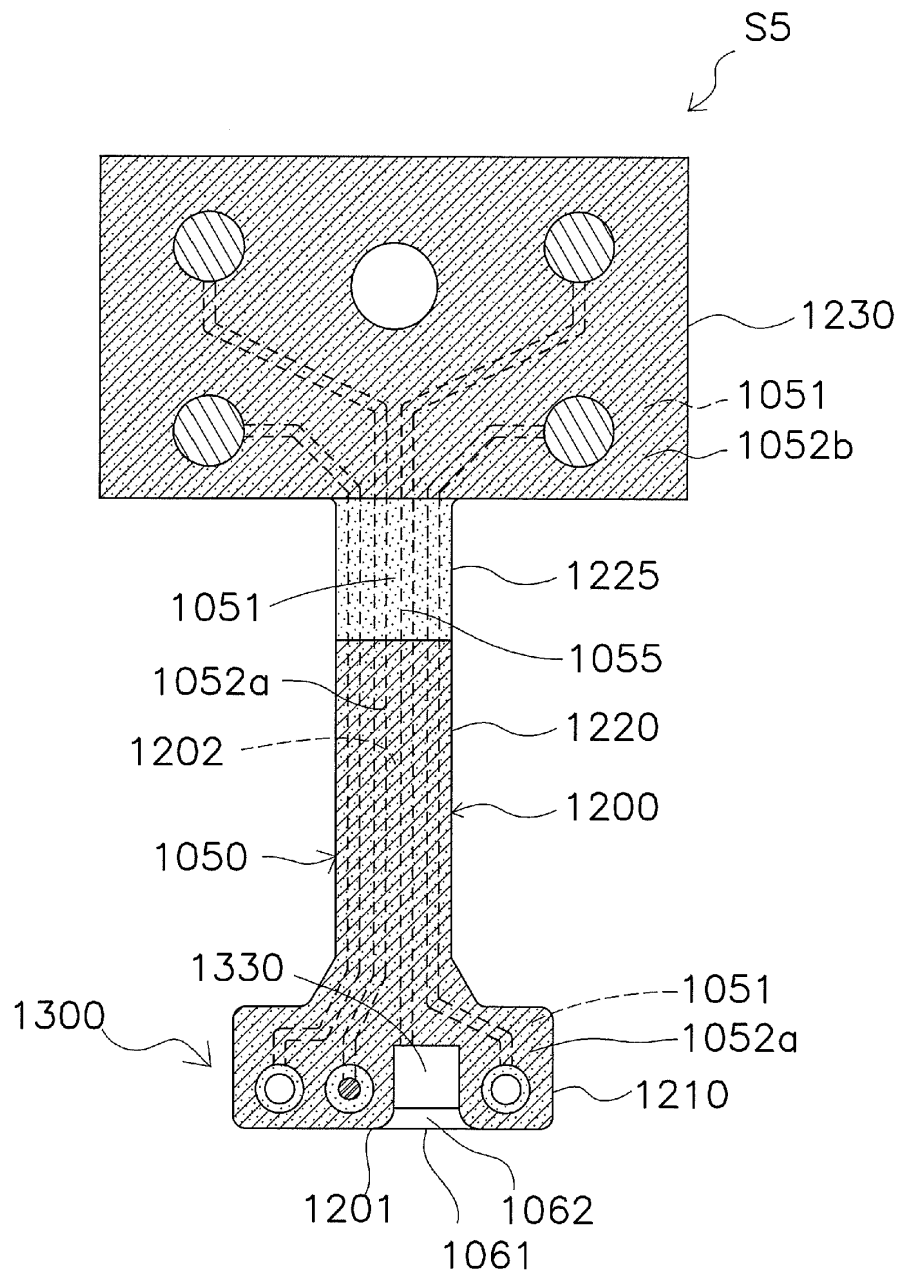
[図49C]



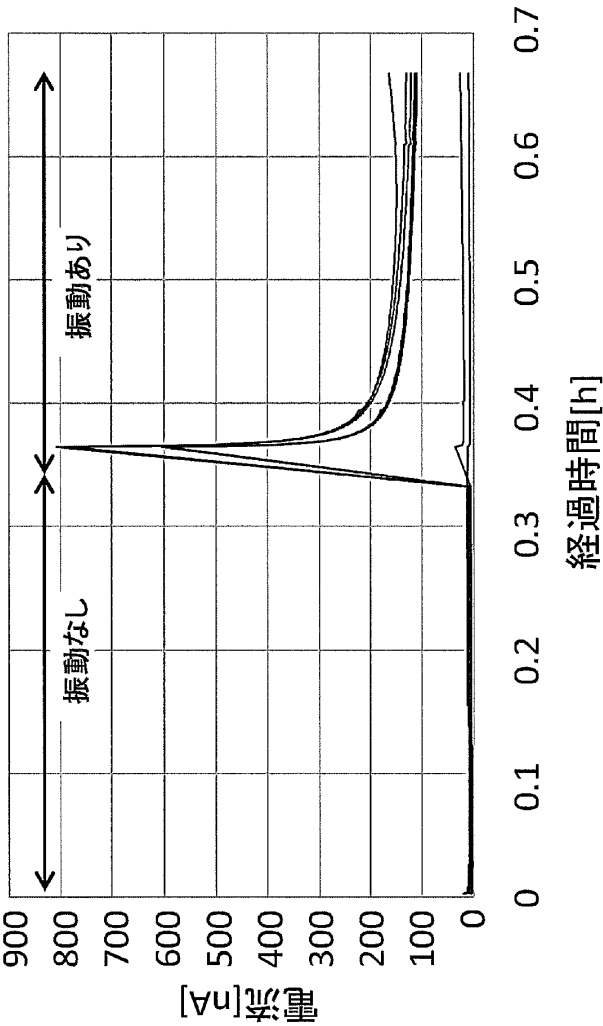
[図49D]



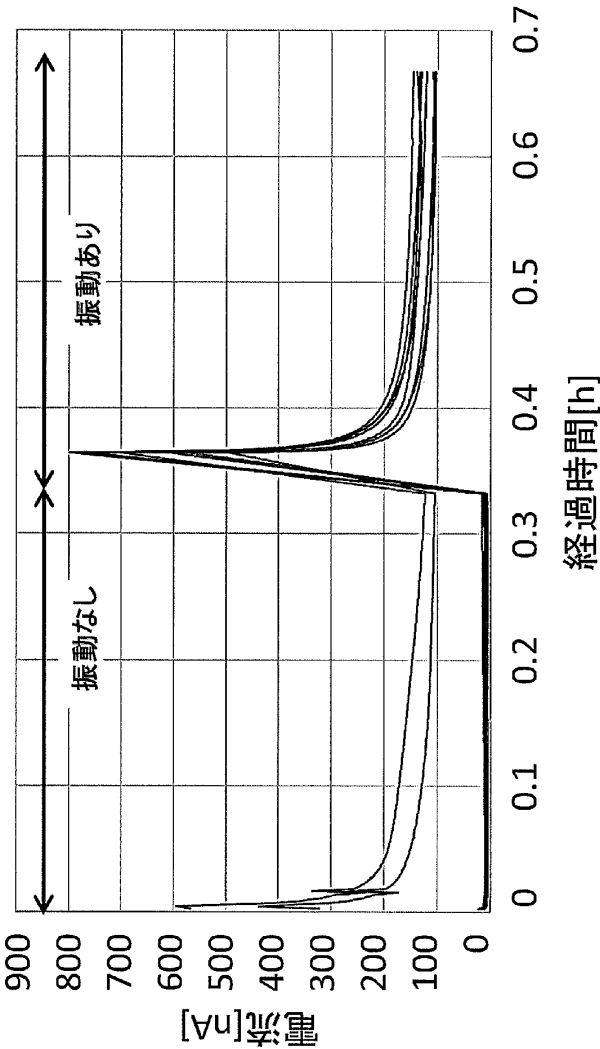
[図49E]



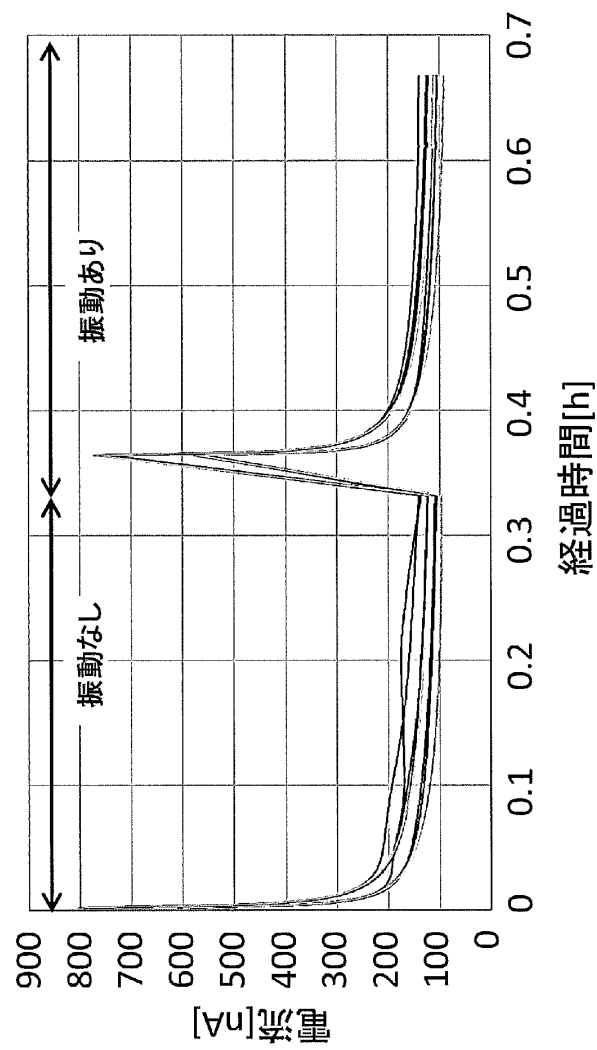
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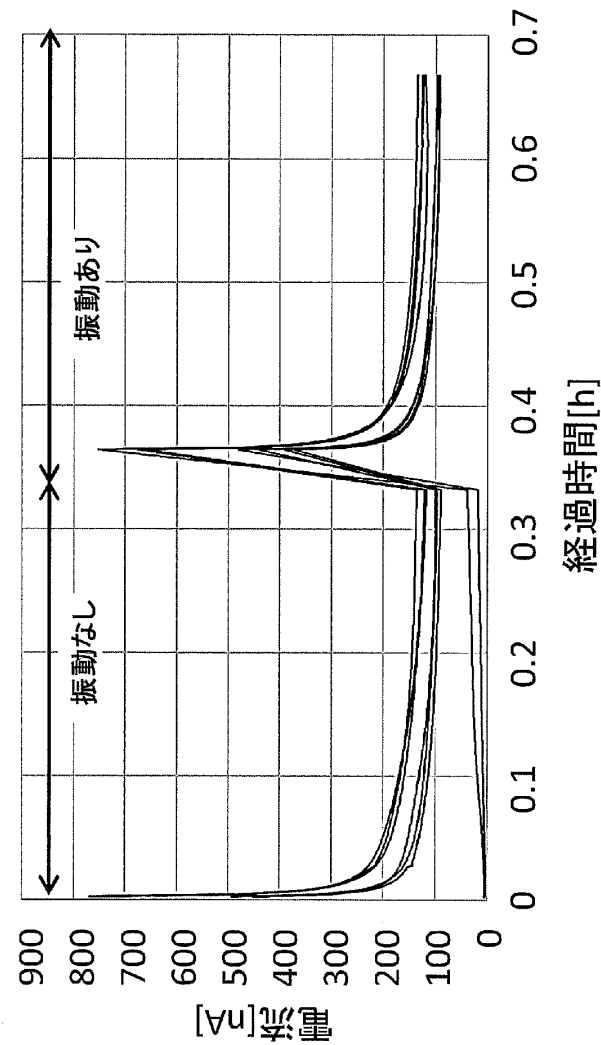
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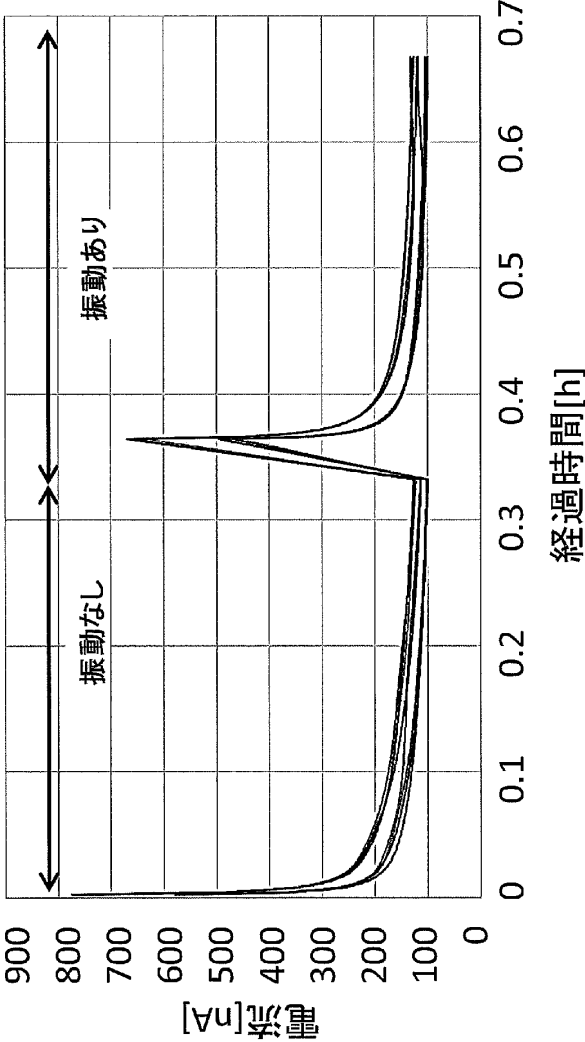
[図50C]



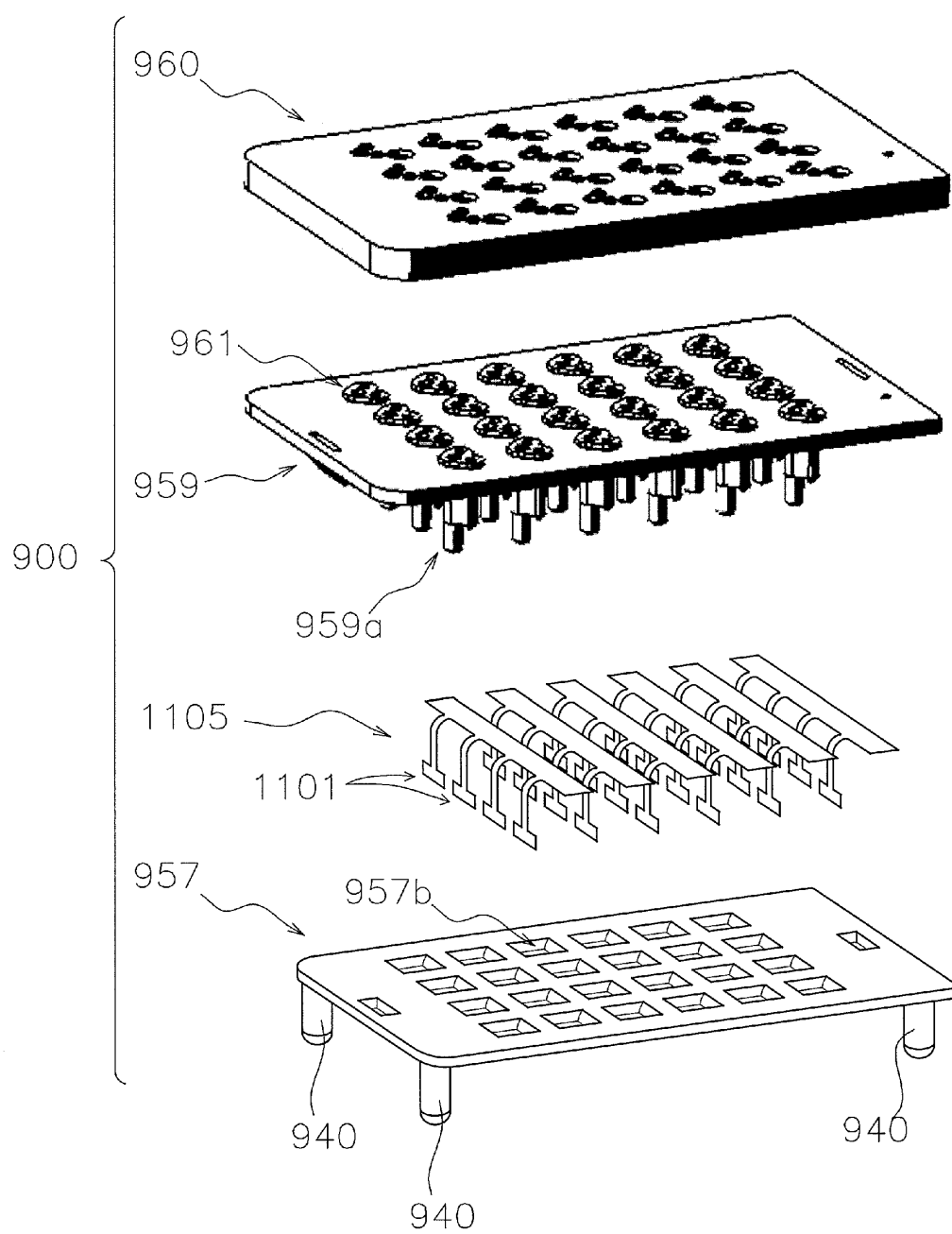
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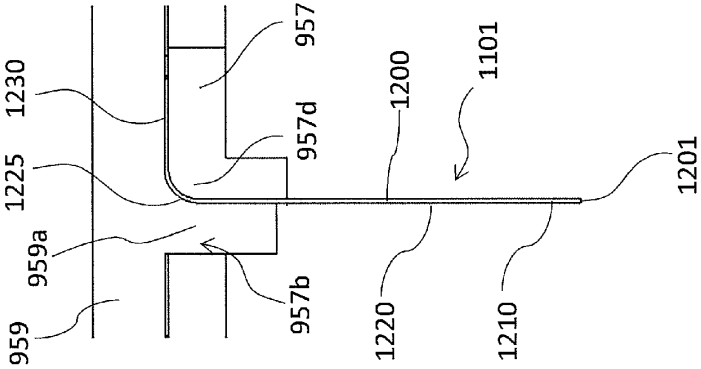
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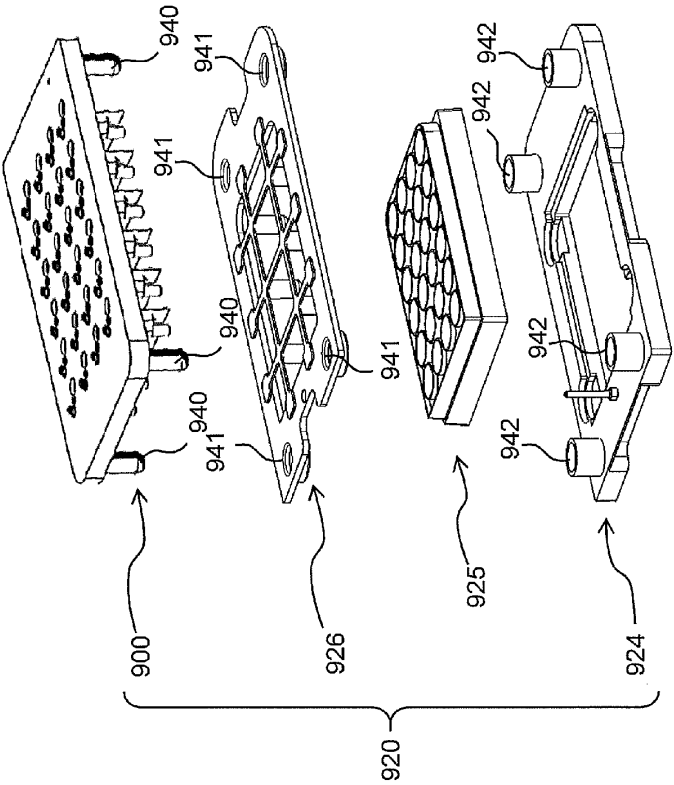
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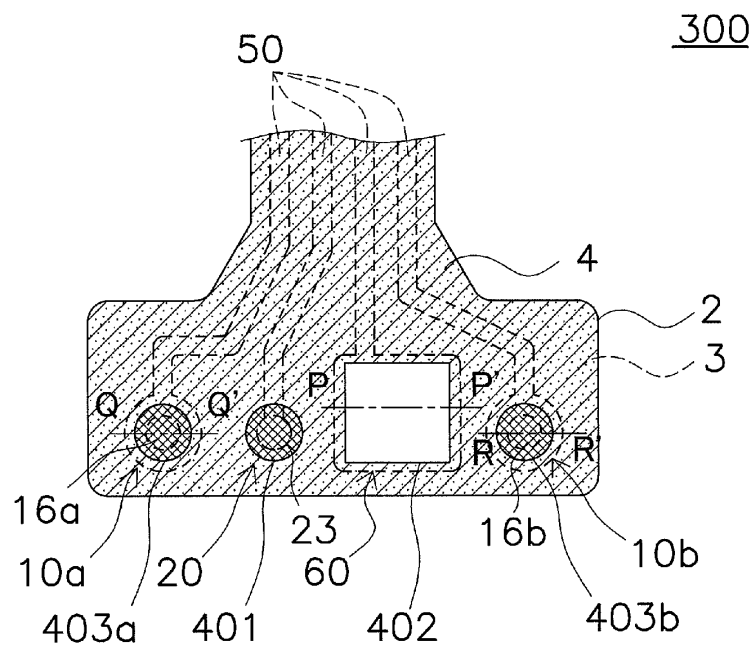
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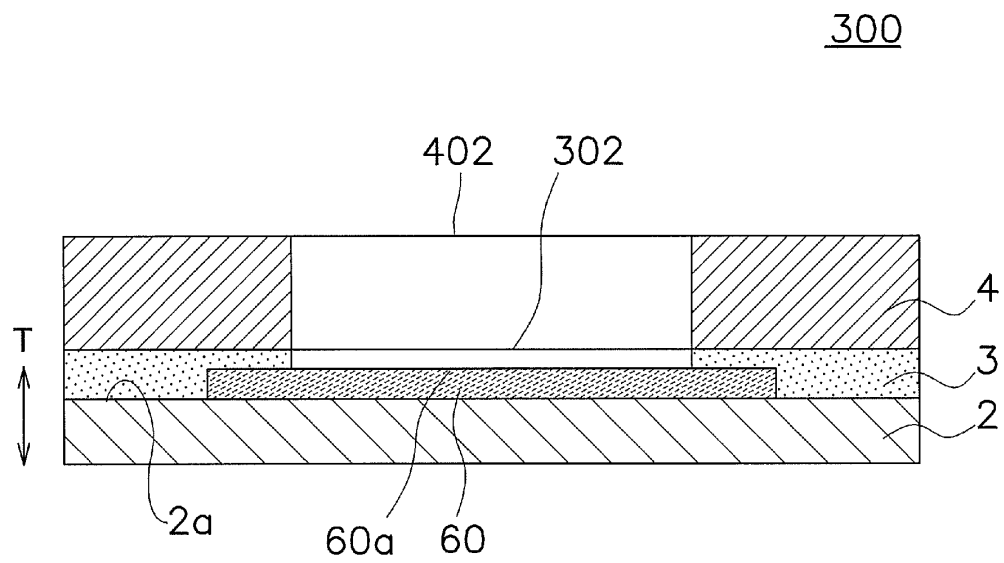
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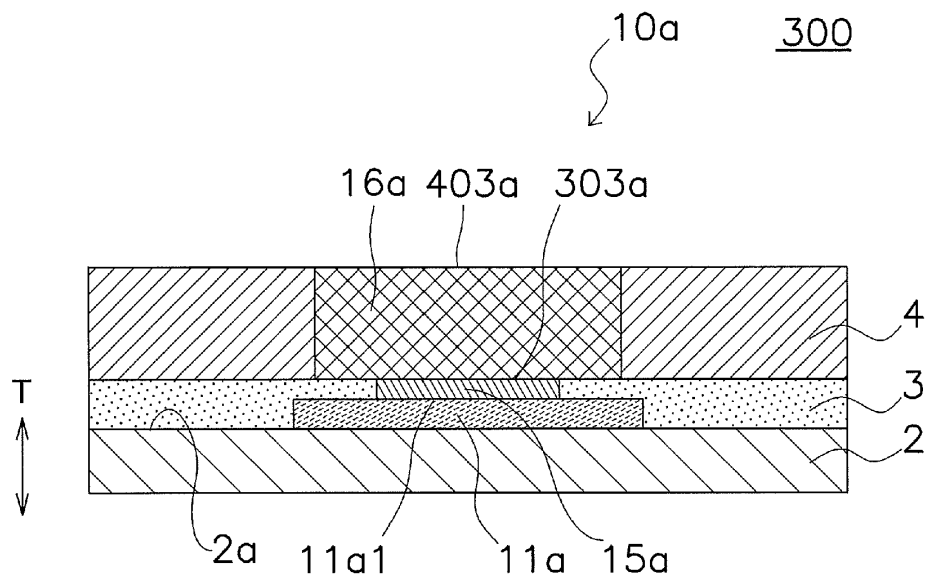
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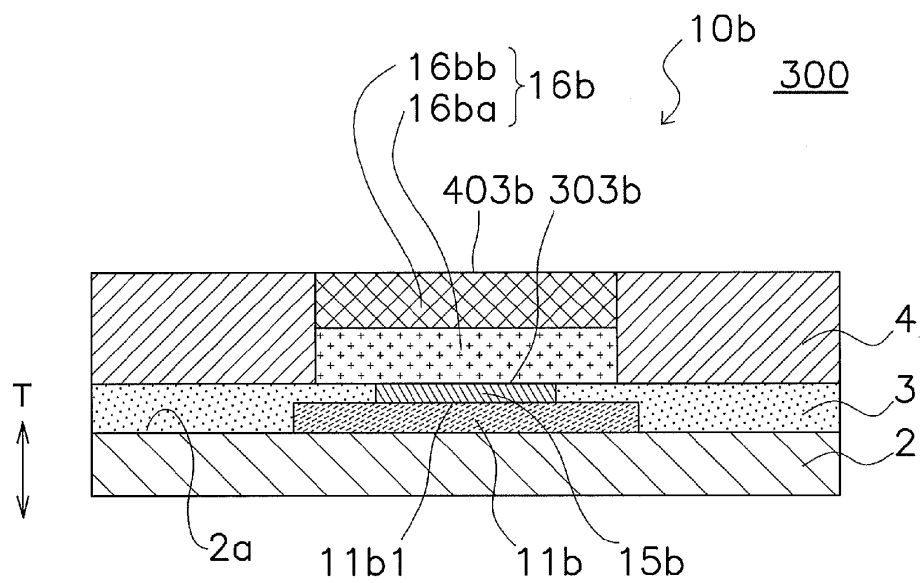
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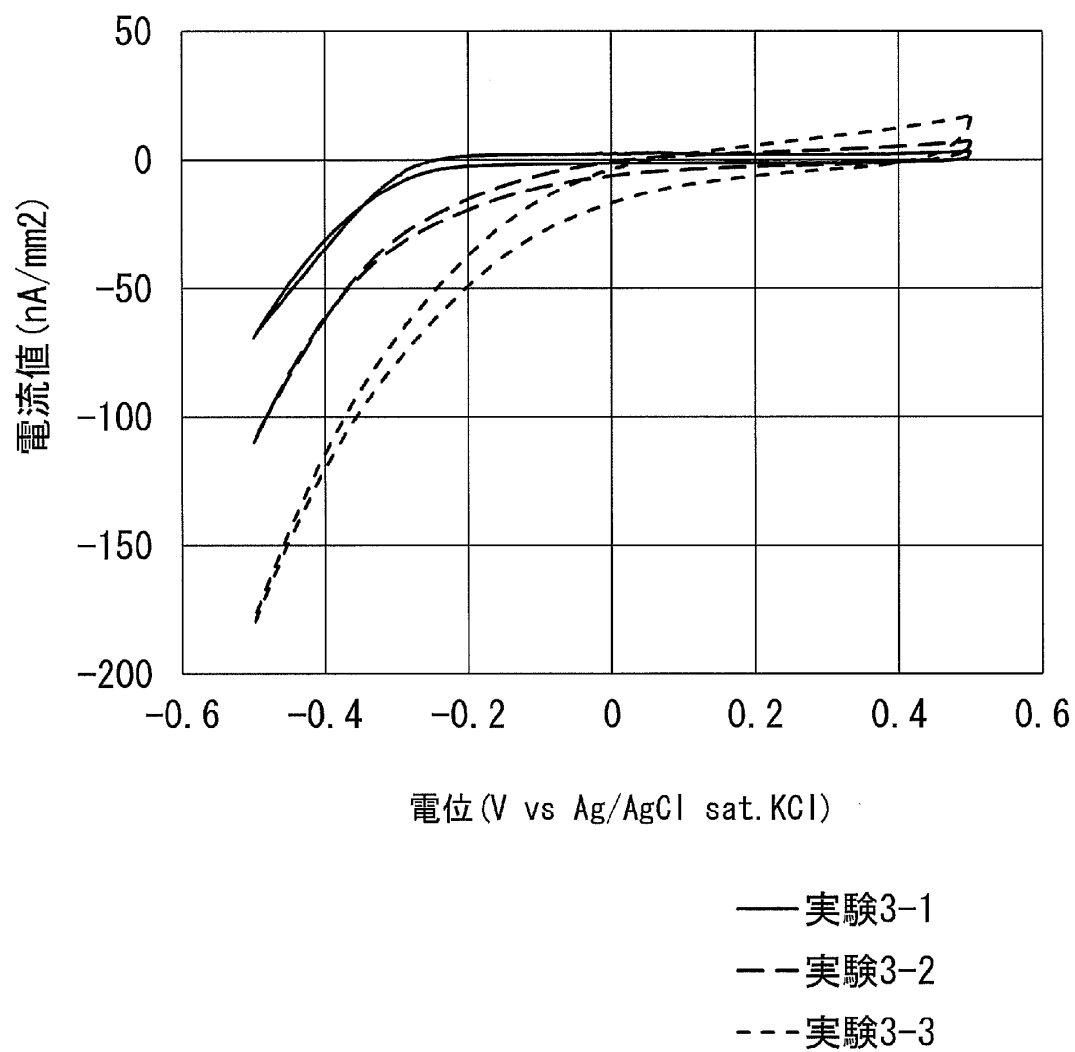
[図56]



[図57]

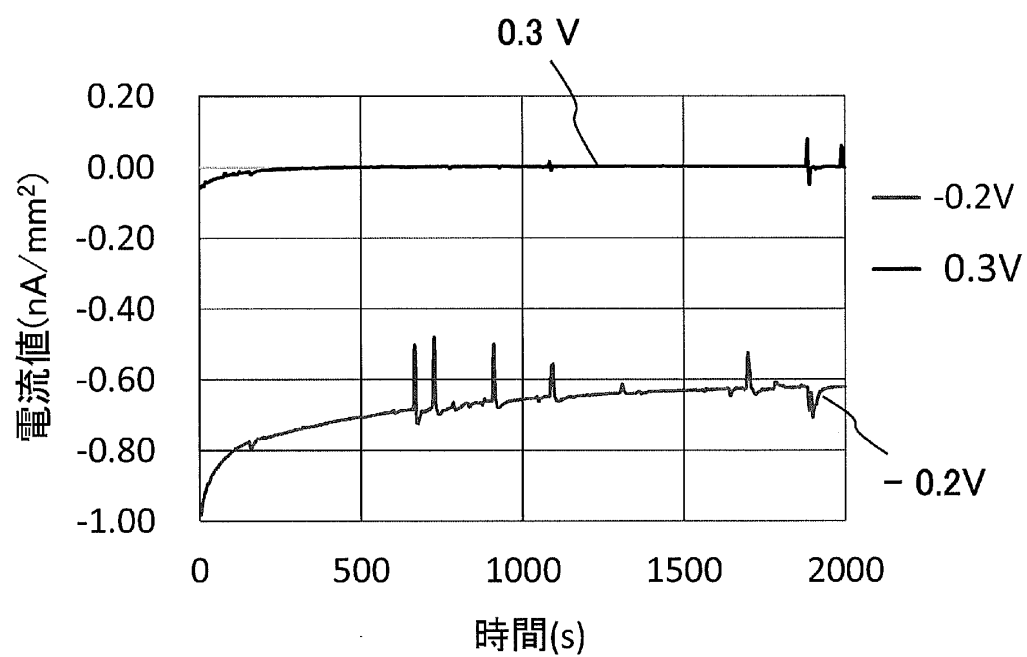


[図58]

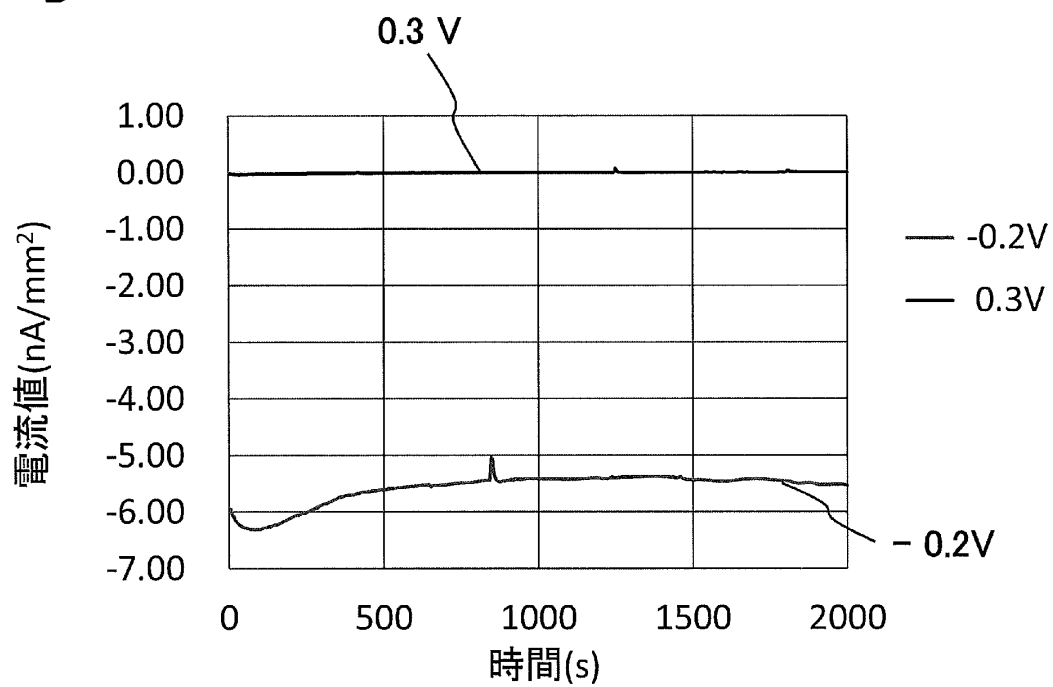


[図59]

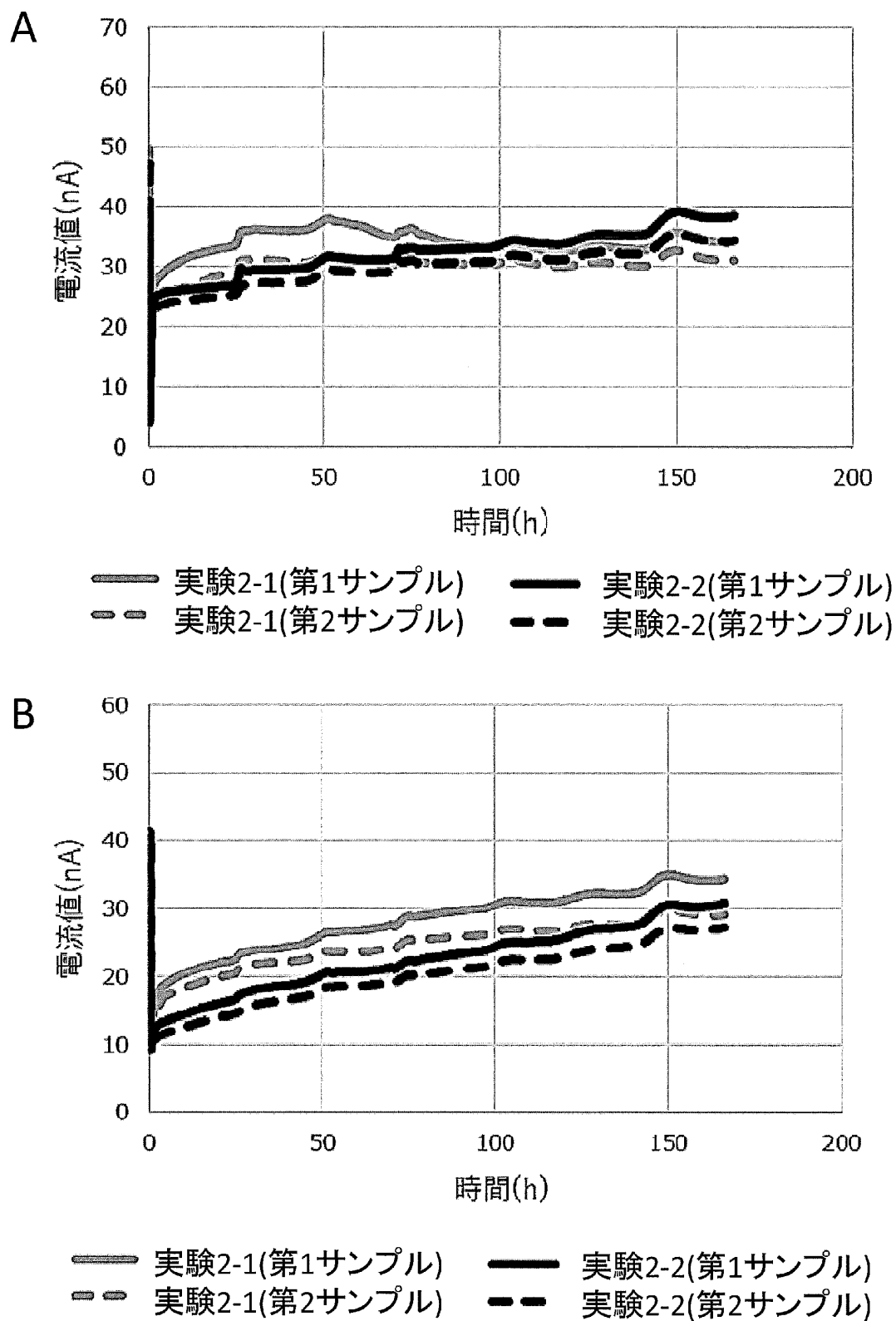
A



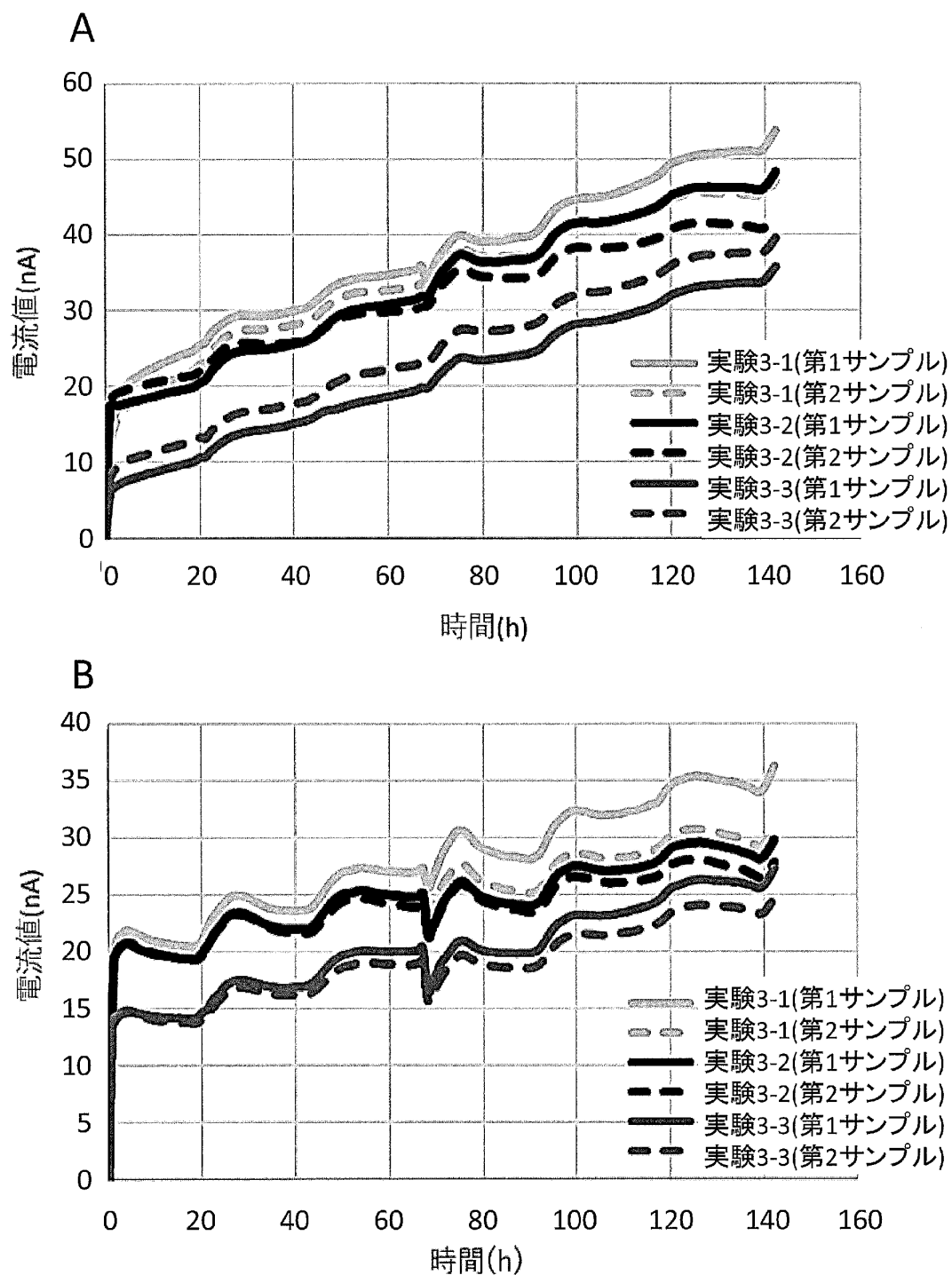
B



[図60]

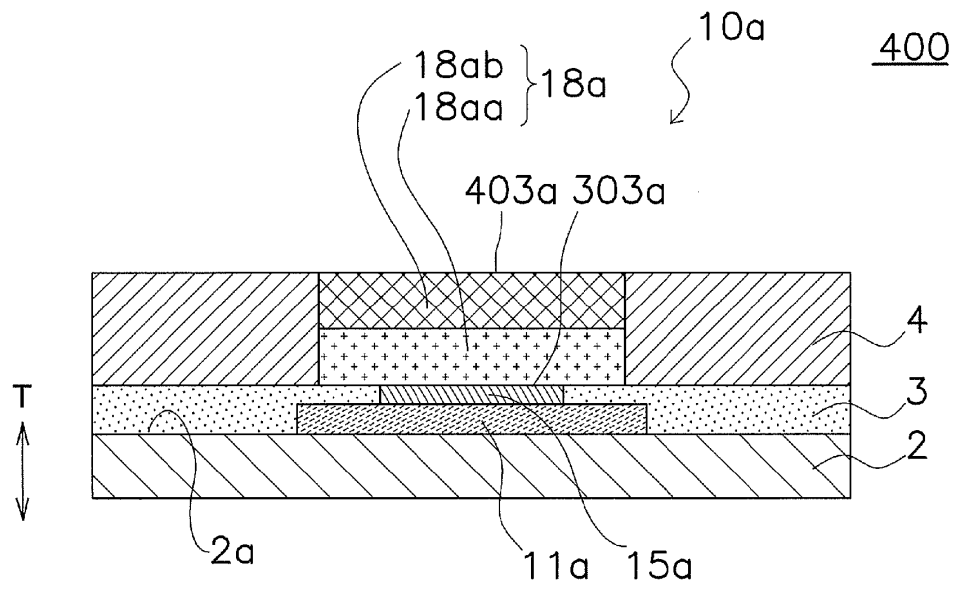


[図61]

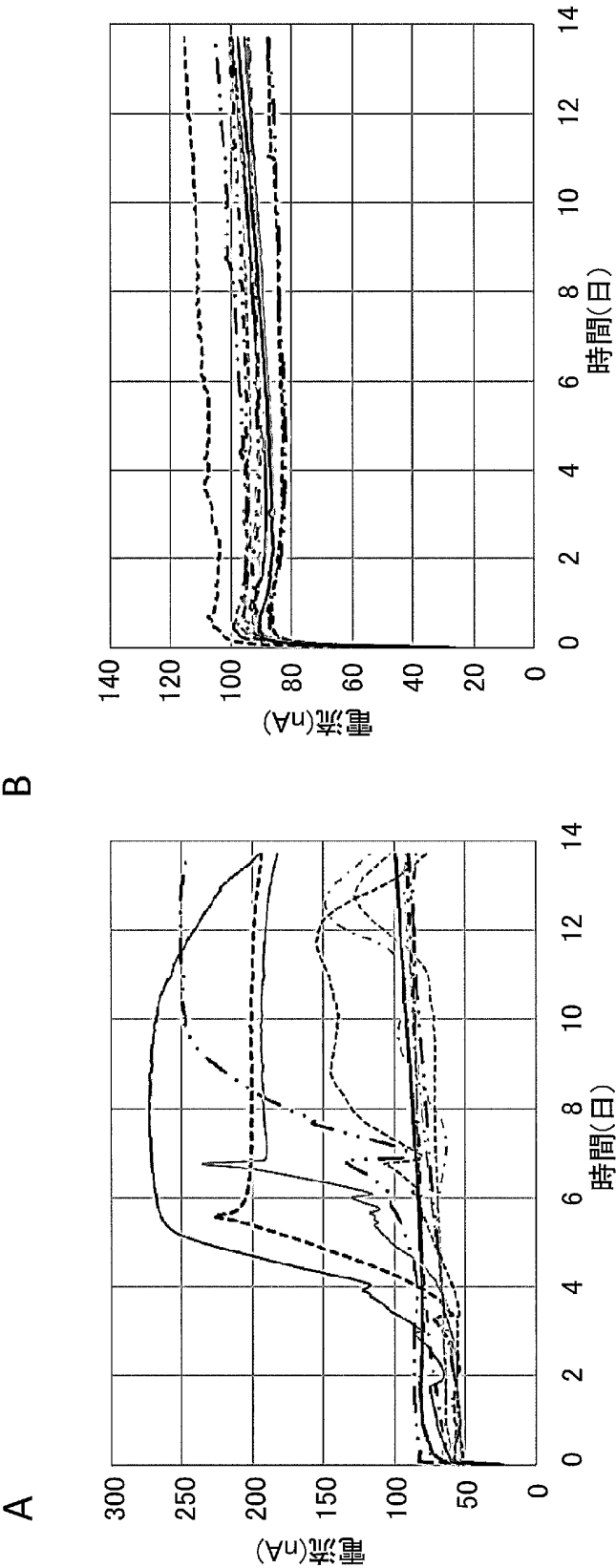


A cross-sectional view of a semiconductor device 400. The device consists of a substrate 2 with a top surface 2a. A thin layer 3 is formed on the top surface 2a. A layer 4 is formed on top of layer 3. A central region of layer 4 is labeled 402, and the surrounding regions are labeled 302. A layer 30 is formed on the top surface 2a, partially overlapping the central region 402. A dimension line T indicates the thickness of the substrate 2.

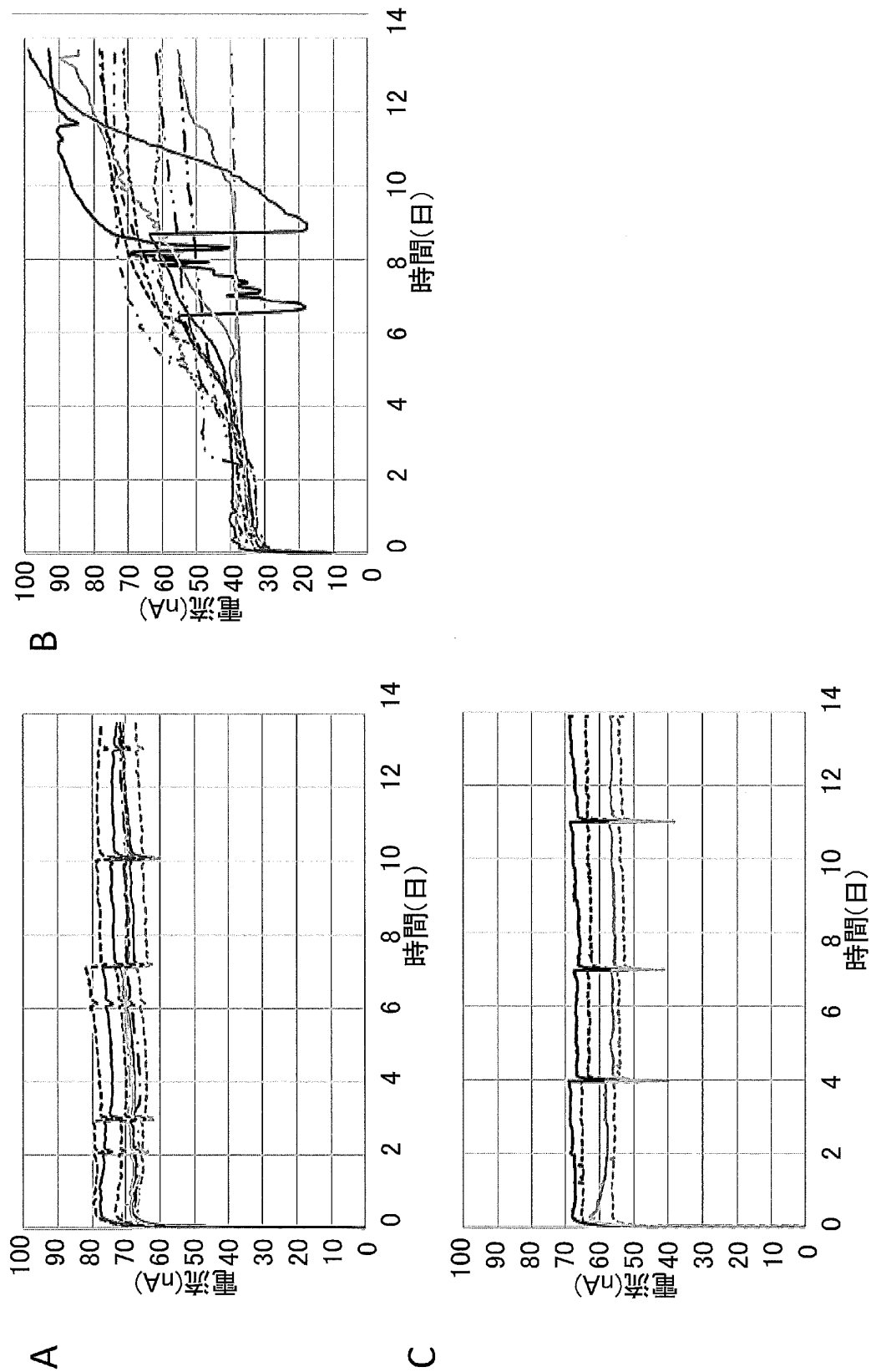
[図64]



[図65]



[図66]



[図67]

