CLAIMS

1. A clock circuit, comprising:

a data strobe clock module, configured to receive a data strobe clock signal and transmit the data strobe clock signal, wherein the data strobe clock signal is used for controlling at least one of receiving or sending of a data signal; and

a system clock module, configured to receive a system clock signal and transmit the system clock signal, wherein the system clock signal is used for controlling receiving of a command signal;

characterized in that the system clock module comprises at least two first signal transmission paths, and is configured to transmit the system clock signal via different first signal transmission paths among the at least two first signal transmission paths based on at least one of: different receiving rates, or sending rates of the data signal;

the data strobe clock module comprises at least two second signal transmission paths, the data strobe clock signal is transmitted via different second signal transmission paths among the at least two second signal transmission paths at different transmission rates, each of the transmission rates corresponds to a respective one of the at least one of: the receiving rates, or the sending rates, and each of the second signal transmission paths is matched with a respective one of the first signal transmission paths; and

wherein the system clock module is configured to transmit, when the data strobe clock signal is transmitted via a second signal transmission path in the second signal transmission paths, the system clock signal via the first signal transmission path matching with the second signal transmission path,

wherein the data strobe clock module further comprises a first data strobe clock transmission circuit and a second data strobe clock transmission circuit, and the first data strobe

clock transmission circuit and the second data strobe clock transmission circuit define the different second signal transmission paths;

wherein the system clock module further comprises a first system clock transmission circuit and a second system clock transmission circuit, and the first system clock transmission circuit and the second system clock transmission circuit define the different first signal transmission paths, and

wherein the first system clock transmission circuit is configured to match the first data strobe clock transmission circuit, and the second system clock transmission circuit is configured to match the second data strobe clock transmission circuit.

2. The clock circuit of claim 1, wherein the data strobe clock module is configured to transmit, when a transmission rate in the transmission rates is greater than or equal to a preset value, the data strobe clock signal through the first data strobe clock transmission circuit, and transmit, when the transmission rate is less than the preset value, the data strobe clock signal through the second data strobe clock transmission circuit.

3. The clock circuit of claim 2, wherein the first data strobe clock transmission circuit comprises a first frequency divider unit; the second data strobe clock transmission circuit comprises a second frequency divider unit; and the first frequency divider unit is configured to divide a frequency of the data strobe clock signal and output at least two frequency-divided data strobe clock signals having different phases, and the second frequency divider unit is configured to divide a frequency of the data strobe clock signal and output at least two frequency-divided data strobe clock signals having different phases.

4. The clock circuit of claim 3, wherein the first frequency divider unit has a first correlation between power consumption and the frequency of the data strobe clock signal, the second frequency divider unit has a second correlation between power consumption and the frequency of the data strobe clock signal, and the first correlation is weaker than the second correlation;

or, the first frequency divider unit has a first anti-interference capability, the second frequency divider unit has a second anti-interference capability, and the first anti-interference capability is stronger than the second anti-interference capability.

5. The clock circuit of claim 3 or 4, wherein the first frequency divider unit comprises a current-mode logic frequency divider circuit, and the second frequency divider unit comprises a complementary metal oxide semiconductor (CMOS) frequency divider circuit.

6. The clock circuit of claim 5, wherein the first data strobe clock transmission circuit further comprises a current-mode logic to CMOS unit, configured to be connected to the current-mode logic frequency divider circuit and output the frequency-divided data strobe clock signals.

7. The clock circuit of claim 5, wherein the second data strobe clock transmission circuit further comprises a current-mode logic to CMOS unit, configured to output the data strobe clock signal to the CMOS frequency divider circuit.

8. The clock circuit of claim 2, wherein each of the first data strobe clock transmission circuit and the second data strobe clock transmission circuit comprises a buffer, configured to buffer and receive the data strobe clock signal.

9. The clock circuit of claim 8, wherein the buffer is a current-mode logic buffer.

10. The clock circuit of claim 2, wherein the system clock module is configured to transmit, when the data strobe clock signal is transmitted through the first data strobe clock transmission circuit, the system clock signal through the first system clock transmission circuit, and

transmit, when the data strobe clock signal is transmitted through the second data strobe clock transmission circuit, the system clock signal through the second system clock transmission circuit.

11. The clock circuit of claim 10, wherein the first system clock transmission circuit comprises a first frequency divider unit model, and the second system clock transmission circuit comprises a second frequency divider unit model; and the first frequency divider unit model is configured to match a clock delay of the first data strobe clock transmission circuit, and the second frequency divider unit model is configured to match a clock delay of the second data strobe clock transmission circuit.

12. The clock circuit of claim 11, wherein the first frequency divider unit model comprises a current-mode logic frequency divider circuit model, and the second frequency divider unit model comprises a complementary metal oxide semiconductor (CMOS) frequency divider circuit model.

13. The clock circuit of claim 12, wherein the first system clock transmission circuit further comprises a current-mode logic to CMOS unit, configured to be connected to the current-mode logic frequency divider circuit model and output the system clock signal.

14. The clock circuit of claim 13, wherein the second system clock transmission circuit further comprises a current-mode logic to CMOS unit, configured to output the system clock signal to the CMOS frequency divider circuit model.

15. The clock circuit of claim 14, wherein each of the first system clock transmission circuit and the second system clock transmission circuit comprises a buffer, configured to buffer and receive the system clock signal.

16. The clock circuit of claim 15, wherein the buffer is a current-mode logic buffer.

17. The clock circuit of claim 10, wherein the data strobe clock module further comprises a first selector circuit, and the first selector circuit is configured to select an output signal of one of the first data strobe clock transmission circuit and the second data strobe clock transmission circuit for output; and the system clock module further comprises a second selector circuit, and the second selector circuit is configured to select an output signal of one of the first system clock transmission circuit and the second system clock transmission circuit for output.

18. The clock circuit of claim 17, further comprising a handshake module, connected to outputs of the first selector circuit and the second selector circuit and configured to determine a phase relationship between the system clock signal and the data strobe clock signal.

19. A memory, comprising:

the clock circuit of any one of claims 1 to 18.