CLAIMS

1. A semiconductor structure, characterized in that the semiconductor structure comprises:

a substrate;

word lines, located in the substrate, wherein each of bit line contact holes is provided between two adjacent word lines;

bit line contact plugs, located in bit line contact holes; and

first isolation layers, located on side walls of the bit line contact holes and covering side walls of the bit line contact plugs;

wherein one of the first isolation layers comprises a silicon nitride layer, and the silicon nitride layer is in contact with one of the bit line contact plugs, the one of the bit line contact plugs is a three-layer structure, comprising a metal material and two layers of polycrystalline silicon; the metal material is sandwiched between the two layers of polycrystalline silicon, and the silicon nitride layer covers the metal material and an upper-layer polycrystalline silicon of the two layers of polycrystalline silicon, but not a lower-layer polycrystalline silicon of the two layers of polycrystalline silicon.

2. The semiconductor structure of claim 1, characterized in that the one of the first isolation layers further comprises a silicon oxide layer, the silicon oxide layer is in contact with the side wall of the bit line contact hole.

3. The semiconductor structure of claim 1, characterized in that a bottom end of the one of the first isolation layers is flush with a bottom end of the one of the bit line contact plugs, and/or, the one of the first isolation layers is not lower than an upper surface of the substrate.

4. The semiconductor structure of claim 1, characterized in that the metal material is not higher than an upper surface of the substrate.

5. The semiconductor structure of claim 1, characterized in that the semiconductor structure further comprises:

second isolation layers, located on the word lines; and

word line surface layers, located in the second isolation layers, the second isolation layers covering side walls and bottom walls of the word line surface layers,

wherein the one of the bit line contact plugs is located between two adjacent second isolation layers.

6. The semiconductor structure of claim 5, characterized in that the semiconductor structure further comprises:

nitride layers, located between the second isolation layers and the word lines.

7. The semiconductor structure of claim 5, characterized in that a bottom end of the one of the first isolation layers is higher than a bottom end of the second isolation layer.

8. The semiconductor structure of claim 1, characterized in that the semiconductor structure further comprises:

a capacitor, located on the substrate.

9. A method for manufacturing a semiconductor structure, characterized in that the method comprises:

providing a substrate;

forming word lines in the substrate, and forming a bit line contact hole between two adjacent word lines;

forming a first isolation layer on a side wall of the bit line contact hole, the first isolation layer comprises a silicon nitride layer; and

forming a bit line contact plug in the first isolation layer, the first isolation layer covering a side wall of the bit line contact plug,

wherein forming the bit line contact plug comprises:

forming a first layer of polycrystalline silicon as a lower-layer polycrystalline silicon in the first isolation layer, the first layer of polycrystalline silicon covering the bit line contact hole;

forming a metal material on the lower-layer polycrystalline silicon; and

forming a second layer of polycrystalline silicon as an upper-layer polycrystalline silicon on the metal material; wherein the silicon nitride layer covers the metal material and the upper-layer polycrystalline silicon, but not the lower-layer polycrystalline silicon.

10. The method for manufacturing the semiconductor structure of claim 9, characterized in that the method, before forming the first isolation layer, further comprises:

forming second isolation layers on the word lines; and

forming word line surface layers in the second isolation layers, the second isolation layers covering side walls and bottom walls of the word line surface layers.

11. The method for manufacturing the semiconductor structure of claim 10, characterized in that forming the first isolation layer comprises:

forming an opening in the substrate, and exposing the second isolation layers, the opening serving as the bit line contact hole; and

forming the first isolation layer on a side wall of the opening.