

ABSTRACT

Disclosed in the embodiments of the present disclosure is a topological structure for an IP core. The topological structure comprises a first topological structure and a second topological structure, wherein the first topological structure comprises a drive chip, multi-level first signal lines and at least two first loads, a signal output end of a previous-level first signal line being connected to signal input ends of two next-level first signal lines which are connected in parallel, a signal input end of a first-level first signal line being connected to a signal output end of the drive chip, and an output end of each last-level first signal line being connected to a first load; and the second topological structure comprises a plurality of branch structures, each of which comprises at least one second load, a signal input end of each branch structure being connected to a signal output end of a last-level first signal line of the first topological structure. A new topological structure is provided for an IP core, so as to realize diversified IP core topological structures to adapt to different requirements.