CLAIMS

WHAT IS CLAIMED IS:

[Claim 1]

A semiconductor structure, comprising:

a substrate, comprising an element region and a peripheral region surrounding the element region;

a semiconductor element, disposed on the substrate in the element region;

an interconnect structure, disposed above the semiconductor element in the element region, and electrically connected to the semiconductor element;

a first power deliver line, disposed above the interconnect structure and electrically connected to a first power source;

a second power deliver line, disposed above the interconnect structure and electrically connected to a second power source;

a first power deliver network structure, disposed between the substrate in the peripheral region and the first power deliver line, and connected to the first power deliver line and a lowest circuit layer of the interconnect structure; and

a second power deliver network structure, disposed between the substrate in the peripheral region and the second power deliver line, and is connected to the second power deliver line and the lowest circuit layer of the interconnect structure,

wherein the first power deliver network structure comprises:

a plurality of first power deliver circuit layers; and

a plurality of first power deliver vias, connected to two adjacent first power deliver circuit layers 110a among the first power deliver circuit layers,

wherein a lowest first power deliver circuit layer of the first power deliver circuit

layers is connected to the lowest circuit layer of the interconnect structure, and the rest of the first power deliver circuit layers are spaced apart from the interconnect structure by a first distance, the first distance being between 1 μm and 10 μm,

wherein the second power deliver network structure comprises:

a plurality of second power deliver circuit layers; and

a plurality of second power deliver vias, connected to two adjacent power deliver circuit layers among the second power deliver circuit layers,

wherein a lowest second power deliver circuit layer of the second power deliver circuit layers is connected to the lowest circuit layer of the interconnect structure, and the rest of the second power deliver circuit layers are spaced apart from the interconnect structure by a second distance, the second distance being between 1 μm and 10 μm.

[Claim 2]

The semiconductor structure according to claim 1, further comprising a first dummy structure, disposed between the first power deliver network structure and the interconnect structure, and electrically separated from the first power deliver network structure and the interconnect structure.

[Claim 3]

The semiconductor structure according to claim 2, wherein the first dummy structure comprises a plurality of first dummy circuit layers.

[Claim 4]

The semiconductor structure according to claim 3, wherein each of the first dummy circuit layers is located at a same horizontal height as the corresponding first power deliver circuit layer.

[Claim 5]

The semiconductor structure according to claim 2, wherein a material of the first dummy structure is the same as a material of the first power deliver network structure.

[Claim 6]

The semiconductor structure according to claim 1, wherein the first power deliver network structure is located in the peripheral region.

[Claim 7]

The semiconductor structure according to claim 1, further comprising a first support structure, disposed between the first power deliver network structure and the substrate.

[Claim 8]

The semiconductor structure according to claim 1, further comprising a second dummy structure, disposed between the second power deliver network structure and the interconnect structure, and electrically separated from the second power deliver network structure and the interconnect structure.

[Claim 9]

The semiconductor structure according to claim 8, wherein the second dummy

structure comprises a plurality of second dummy circuit layers.

[Claim 10]

The semiconductor structure according to claim 9, wherein each of the second dummy circuit layers is located at a same horizontal height as the corresponding second power deliver circuit layer.

[Claim 11]

The semiconductor structure according to claim 8, wherein a material of the second dummy structure is the same as a material of the second power deliver network structure.

[Claim 12]

The semiconductor structure according to claim 1, wherein the second power deliver network structure is located in the peripheral region.

[Claim 13]

The semiconductor structure according to claim 1, further comprising a second support structure, disposed between the second power deliver network structure and the substrate.

[Claim 14]

The semiconductor structure according to claim 1, wherein a distance between the first power deliver network structure and the second power deliver network structure is between 10 μm and 1000 μm.

[Claim 15]

A semiconductor structure, comprising:

a substrate, comprising an element region and a peripheral region surrounding the element region;

a semiconductor element, disposed on the substrate in the element region;

an interconnect structure, disposed in the element region, located above the semiconductor element, and electrically connected to the semiconductor element;

a first power deliver line, disposed above the interconnect structure and electrically connected to a first power source;

a second power deliver line, disposed above the interconnect structure and electrically connected to a second power source;

a first power deliver network structure, disposed in the interconnect structure, and connected to the first power deliver line and a lowest circuit layer of the interconnect structure; and

a second power deliver network structure, disposed in the interconnect structure, and is connected to the second power deliver line and the lowest circuit layer of the interconnect structure,

wherein the first power deliver network structure comprises:

a plurality of first power deliver circuit layers; and

a plurality of first power deliver vias, connected to two adjacent first power deliver circuit layers 110a among the first power deliver circuit layers,

wherein a lowest first power deliver circuit layer of the first power deliver circuit layers is connected to the lowest circuit layer of the interconnect structure, the rest of the first power deliver circuit layers are spaced apart from the interconnect structure by a

first distance and the first distance is between 1 μm and 10 μm, and

wherein the second power deliver network structure comprises:

a plurality of second power deliver circuit layers; and

a plurality of second power deliver vias, connected to two adjacent power deliver circuit layers among the second power deliver circuit layers,

wherein a lowest second power deliver circuit layer of the second power deliver circuit layers is connected to the lowest circuit layer of the interconnect structure, the rest of the second power deliver circuit layers are spaced apart from the interconnect structure by a second distance and the second distance is between 1 μm and 10 μm.