

MODULAR DESIGN METHOD OF A DATA ACQUISITION AND PROCESSING APPARATUS BASED ON FPGA AND SINGLE-BOARD COMPUTER, AND A SUCH APPARATUS DESIGNED WITH THE METHOD

5

Technical Field

Embodiments of the invention relate to modular design method of a data acquisition and processing apparatus based on FPGA and single-board computer, and a data acquisition and processing apparatus designed with the this method.

10

Background

15

A commonly used data acquisition and processing apparatus design method (Method-A) is designing a data acquisition (DAQ) card with a FPGA device as the core controller and processor, and with a USB or/and Ethernet port, or PCIe interface on the card for data and instruction input and output. A such DAQ card with USB or/and Ethernet port is usually housed in an enclosure and made into a box-type data acquisition card. A such box-type DAQ card is connected to a computer through the USB or Ethernet port to form a complete data acquisition and processing equipment. A such DAQ card with PCIe interface is usually made into a plug-in card, and is plugged in a PCIe expansion slot on the motherboard of a desktop computer to form a complete data acquisition and processing equipment. When designing any of the above DAQ cards, a USB, Ethernet or PCIe interface circuitry and associated firmware/software must be involved. When using such a data acquisition card, an external computer is required, which is not cost-effective and even is not allowed by installation conditions in some application scenarios.

30

Another commonly used design method (Method-B) is using a SoC device, like the Zynq series SoC from AMD | Xilinx, which integrates FPGA and CPU in a single chip, as core controller and processor to design an apparatus with both data acquisition and data processing functionalities, which can be used without an external computer. However, such a SoC is often complex and difficult to design with: not only is its circuit board difficult to design, but also special low layer firmware/software as well as a specially tailored operating system have to be made for it with a series of special tools. Long-term study and a lot of practice are needed to master and use these tools well. All these make the design with such a SOC a time and money consuming work. The combination of FPGA and CPU inside such a SoC is fixed -- later on, when the computing capability of an apparatus designed with such SoC needs upgrade, the SoC on the circuits of the apparatus has to be replaced and the circuits has to be modified or re-designed, which will be another time and money consuming work.

45

This invention presents a modular design method for designing a data acquisition and processing apparatus using a FPGA device and a single-board computer (SBC) with general-purpose input-output (GPIO) connector. This method has various advantages over the above Method-A and Method-B. Compared with method A, a DAQ module designed with this method does not need USB, Ethernet or PCIe circuits, and therefore is more easily to design and is lower in cost; an apparatus designed with this method is self-integrated with DAQ and computing capabilities, requires no additional computer for operation and is therefore suitable for application scenarios where using additional computers is not

50

economical viable or technically allowable. Compared with Method-B, this method can greatly reduce the complexity and workload of the design work. As there are vast varieties of ready-made low cost high performance SBCs and ready-made open source operating systems for these SBCs available on the market, the design with this method may only relate to designing a DAQ module and necessary library and application software. The flexibility in choosing a right performance FPGA and a right performance SBC may result in better cost-effective solutions. Upgrading of the computing capability of an apparatus designed with this method can be easy -- only relate to replacing a SBC.

Summary

According to one embodiment, a modular design method of data acquisition and processing apparatus based on FPGA and single-board computer is provided. The method comprises:

separating the circuitry of the data acquisition and processing apparatus to be designed into two function modules: a computing module and a data acquisition (DAQ) module;

adopting a single-board computer (SBC) with a general purpose input-output (GPIO) connector as a computing module;

adopting a data acquisition (DAQ) module with a FPGA device as its core processor and controller, and with an IO connector corresponding to a GPIO connector on an aforesaid SBC;

electrically connecting an aforesaid SBC and an aforesaid DAQ module via the above mentioned connectors on them;

stipulating a communication protocol that governs the data and instruction exchanges between the aforesaid two connected modules;

designing FPGA programming code (Intellectual Property, IP) that controls the operation of various relative circuits of the DAQ module, processes the acquired data as required and implements the aforesaid communication protocol in the aforesaid FPGA, and loading this IP onto the aforesaid DAQ module;

designing software library functions that implements the aforesaid communication protocol on the aforesaid SBC;

designing software programs that run on the SBC and carry out multiple tasks, including: exchanging instruction and data with the DAQ module by calling the aforesaid library functions, processing data coming from the DAQ module as required, accomplishing other functionalities as required;

wherein adopting a single-board computer (SBC) is one of the following activities:

adopting a commercially available ready-made SBC, and
adopting a SBC specially designed for this apparatus;

wherein adopting a data acquisition (DAQ) module is one of the following activities:
adopting a commercially available ready-made DAQ module, and
adopting a DAQ module specially designed for this apparatus;

5

According to one embodiment of this invention, a such apparatus designed with the method is presented. The apparatus comprises:

10 a commercially available ready-made SBC with a 2.54mm-pitch 40-pin male DIP connector which has a plurality number of its pins each coupling to a GPIO pin of the CPU of the SBC, and

15 a specially designed DAQ module with a FPGA device as its core processor and controller, and a 2.54mm-pitch 40-pin female DIP connector which has a plurality number of its pins each coupling to an IO pin of a FPGA device of the DAQ module;

wherein the above SBC and DAQ module are configured to connect to each other by plugging-in the aforesaid male and female connectors together, each pair of the corresponding pins on the above two connected connectors are electrically connected;

20

wherein the DAQ module further comprising:

analogue signal receiving and adjusting circuits configured receiving and adjusting analogue signals,

25 analogue to digital converting (ADC) circuits configured receiving the adjusted analogue signals from the preceding connected analogue signal receiving and adjusting circuits, and converting the adjusted analogue signals into digital signals (data),

flash memory configured storing the FPGA IP,

30 clock generating circuits configured providing operating clock to the FPGA device and various digital circuits on the DAQ module,

RAM configured being connected to the FPGA device and providing additional data memory,

power supply circuits,

FPGA IP loaded in the flash memory on the DAQ module;

35

wherein the SBC further comprising:

Linux operating system,

software library functions, and

application software programs.

40

Brief Description of Drawings

45 Embodiments of the invention are disclosed hereafter with reference to the drawings, in which:

Figure 1A is a block diagram illustrating a computing module (SBC, Module-A) with a GPIO connector (Conn-1), a DAQ module (Module-B) with an IO connector (Conn-2), as well
50 as the inter-connection manner of Module-A and Module-B --- directly plugging-in the Conn-1 and Conn-2 together.

Figure 1B is a block diagram illustrating a computing module (SBC, Module-A) with a GPIO connector (Conn-1), a DAQ module (Module-B) with an IO connector (Conn-2), as well as the inter-connection manner of Module-A and Module-B -- connecting the connectors Conn-1 and Conn-2 with a multiple-conductor flat cable.

Figure 2 illustrates the corresponding relationship of pin positions between Conn-1 and Conn-2 by taking a pair of corresponding pins as an example.

Figure 3 illustrates the steps of the design method of this invention.

Detailed Description

In the following description, numerous specific details are set forth in order to provide a thorough understanding of various illustrative embodiments of the invention. It will be understood, however, to one skilled in the art, that embodiments of the invention may be utilized and structural, logical and electrical changes may be made without departing from the scope of the invention. In the drawings, like reference numerals refer to same or similar functionalities or features throughout the several views. Some well known, common and/or basic electronic circuit knowledge, information and details have not been described in order not to unnecessarily obscure pertinent aspects of embodiments being described.

Figure 1A and Figure 1B illustrate the block diagrams of some embodiments of the invention. In either Figure 1A or 1B, the circuitry comprises two modules: Module-A is a SBC with a GPIO connector (Conn-1), which is a 2.54mm-pitch 40-pin male DIP connector; Module-B is a DAQ module with an IO connector (Conn-2), which is a 2.54mm-pitch 40-pin female DIP connector. In Figure-1A, Module-A and Module-B are connected by directly plugging-in the Conn-1 and Conn-2 on them together. In Figure-1B, Module-A and Module-B are connected by a multiple-conductor flat cable. When connected in any of the ways described above, the corresponding pins on Conn-1 and Conn-2 are electrically connected.

As illustrated in Figure 1A and 1B, each GPIO pin of Conn-1 is configured to couple to a GPIO pin of the CPU on a the SBC (Module-A).

Also as illustrated in Figure 1A and 1B, each IO pin of Conn-2 is configured to couple to an IO pin of a FPGA device on the DAQ module (Module-B) via a serially connected resistor.

Also as illustrated in Figure 1A and 1B, a computing module (SBC, Module-A), further comprising:

- Linux operating system (OS),
- software library functions, and
- application software programs.

Also as illustrated in Figure 1A and 1B, a DAQ module (Module-B), besides the FPGA device and IO connector Conn-2, further comprising:

- analogue signal receiving and adjusting circuits (201),
- analogue to digital converting (ADC) circuits (202),
- flash memory (203),
- clock generating circuits (204),

RAM (205),
power supply circuits (206),

5 wherein circuits 201 are configured to receive analogue signals, amplify/attenuate and filter the received analogue signals to an amplitude and frequency range suitable for the succeeding ADC circuits to perform ADC, in one embodiment, the amplitude range is -1v ~ +1v, the frequency range is 50kHz~50MHz;

10 wherein the ADC circuits (202) are configured to couple to circuits 201, receive the adjusted analogue signals from circuits 201 and convert the received analogue signals into digital signals (data) at a specific converting rate, in one embodiment, the converting rate is 100 MSPS (Mega Samples Per Second);

15 wherein the FPGA device is configured to control the operations of various circuits on the DAQ module (Module-B), pick up the digital signals (data) from the ADC circuits (202), process the digital signals (data) as necessary and required, and exchange data and instructions with the connected SBC (Module-B);

20 wherein the flash memory (203) is configured to be connected with the FPGA and to store the FPGA programming code (intellectual Property, IP);

25 wherein the clock generating circuits (204) are configured to provide operating clock to the FPGA device and various digital circuits on the DAQ module, in one embodiment, the clock rate is 100 MHz;

wherein the RAM (205) is configured to be connected to the FPGA device and provide additional data memory;

30 wherein the power supply circuits (206) are configured to provide power supplies of various voltages to the circuits on the DAQ module (Module-B), and in one embodiment, 5V power to the SBC (Module-A);

35 Figure 2 illustrates the correspondence relationship between the pins on Conn-1 and Conn-2 by taking a pair of corresponding pins as an example. When Module-A and Module-B are connected in either manners as showed in Figure 1A and Figure 1B, the corresponding pins on Conn-1 and Conn-2 are electrically connected.

Figure 3 illustrates the steps of the design method of this invention.

40 It is to be understood that the embodiments and features described above should be considered exemplary and not restrictive. Many other embodiments will be apparent to those skilled in the art from consideration of the specification and practice of the invention. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.
45 Furthermore, certain terminology has been used for the purposes of descriptive clarity, and not to limit the disclosed embodiments of the invention.

Claims

1. A modular design method of data acquisition and processing apparatus based on FPGA and single-board computer, the method comprising:

5 separating the circuitry of the data acquisition and processing apparatus to be designed into two function modules: a computing module and a data acquisition (DAQ) module;

 adopting a single-board computer (SBC) with a GPIO connector as a computing module;

10 adopting a data acquisition (DAQ) module with a FPGA device as its core processor and controller, and an IO connector corresponding to the GPIO connector on an aforesaid SBC;

 electrically connecting an aforesaid SBC and an aforesaid DAQ module via the above mentioned connectors on them;

15 stipulating a communication protocol that governs the data and instruction exchanges between the aforesaid two connected modules;

 designing FPGA programming code (Intellectual Property, IP) that controls the operation of various relative circuits of the DAQ module, processes the acquired data as required and implements the aforesaid communication protocol in the aforesaid FPGA, and loading this IP onto the aforesaid DAQ module;

20 designing software library functions that implements the aforesaid communication protocol on the aforesaid SBC;

 designing software programs that run on the SBC and carry out multiple tasks, including: exchanging instruction and data with the DAQ module by calling the aforesaid library functions, processing data coming from the DAQ module as required, accomplishing other functionalities as required;

 wherein adopting a single-board computer (SBC) is one of the following activities:

30 adopting a commercially available ready-made SBC, and
 adopting a SBC specially designed for this apparatus;

 wherein adopting a data acquisition (DAQ) module is one of the following activities:

 adopting a commercially available ready-made DAQ module, and
 adopting a DAQ module specially designed for this apparatus;

35

2. The method of claim 1, wherein adopting a single-board computer (SBC) with a GPIO connector, the GPIO connector is configured with:

40 a first group of plurality number of pins (GPIO pins) each electrically coupling to a GPIO pin of the CPU on the SBC,

 a second group of plurality number of pins electrically connected to the ground of the SBC circuitry,

 a third group of plurality number of pins each electrically connected to one of the various power supply voltages of the SBC circuitry.

45

3. The method of claim 1, wherein adopting a data acquisition (DAQ) module with a FPGA device as its core processor and controller, and an IO connector ..., the IO connector is configured with:

50 a first group of plurality number of pins (IO pins) each electrically coupling to an IO pin of the FPGA device directly or via resistors,

a second group of plurality number of pins electrically connected to the ground of the DAQ module circuitry,

a third group of plurality number of pins each electrically connected to one of the various power supply voltages of the DAQ module circuitry.

5

4. The method of claim 1 and 3, wherein a DAQ module further including:

analogue signal receiving and adjusting circuits configured to receive and adjust analogue signals,

10 analogue to digital converting (ADC) circuits configured to receive the adjusted analogue signals from the preceding connected analogue signal receiving and adjusting circuits, and convert the adjusted analogue signals to digital signals (data),

flash memory configured to store FPGA IP,

clock generating circuits configured to provide operating clock to the FPGA device and various digital circuits on the DAQ module,

15 RAM configured to be connected to the FPGA device and provide additional data memory,

power supply circuits, and

FPGA IP loaded in the flash memory on the DAQ module.

20 5. The method of claim 1 to 4, wherein electrically connecting an aforesaid SBC and an aforesaid DAQ module via the above mentioned connectors on them, electrically connecting includes:

connecting a GPIO connector on a SBC and an IO connector on a DAQ module by directly plugging-in the connectors thereof together, or

25 connecting a GPIO connector on a SBC and an IO connector on a DAQ module with a cable,

30 wherein in each connecting manner above, each IO pin on an IO connector on a DAQ module is electrically connected to a GPIO pin on a GPIO connector on a SBC, each ground pin on an IO connector on a DAQ module is electrically connected to a ground pin on a GPIO connector on a SBC, each power pin on an IO connector on a DAQ module is electrically connected to a power pin of the same voltage on a GPIO connector on a SBC.

6. A such apparatus designed with the method, comprises:

35 a commercially available ready-made SBC with a GPIO connector, and

a specially designed DAQ module with a FPGA chip as its core processor and controller, and an IO connector.

7. According to claim 6, wherein a GPIO connector is a 2.54mm-pitch 40-pin male DIP connector and is further configured comprising:

40 28 number of GPIO pins each coupling to a GPIO pin of a CPU on the SBC,

8 number of ground pins connecting to the ground of the SBC circuits,

2 number of 5V power pins connecting to the 5V power of the SBC circuits, and

2 number of 3.3V power pins connecting to the 3.3V power of the SBC circuits.

45 8. According to claim 6 and 7, wherein an IO connector is a 2.54mm-pitch 40-pin female DIP connector and is further configured comprising:

26 number of IO pins each coupling to an IO pin of a FPGA device on the DAQ module, and locating on a position on the IO connector that is corresponding to the position of a GPIO pin on the GPIO connector of the SBC,

8 number of ground pins each electrically connecting to the ground of the DAQ module circuits, and locating on a position on the IO connector that is corresponding to the position of a ground pin on the GPIO connector of a SBC,

5 2 number of 5V power pins each locating on a position on the IO connector that is corresponding to the position of a 5v power pin on the GPIO connector of a SBC, and
4 number of unconnected pins.

10 9. According to claim 6 to 8, an aforesaid SBC and an aforesaid DAQ module are configured to be connect with each other by plugging the GPIO connector on an aforesaid SBC in the IO connector on an aforesaid DAQ module, and through the plugging-in connection thereof, each pin on the IO connector electrically connects a corresponding pin on the GPIO connector (pin-to-pin connection).

15 10. According to claim 6, 8 and 9, wherein a DAQ module, besides a FPGA device and an IO connector, further comprising:

analogue signal receiving and adjusting circuits,
analogue to digital converting (ADC) circuits,
flash memory,
clock generating circuits,
20 RAM,
power supply circuits,

25 wherein the analogue signal receiving and adjusting circuits are configured to receive analogue signals, amplify/attenuate and filter the received analogue signals to an amplitude and frequency range suitable for the succeeding ADC circuits to perform ADC;

30 wherein the ADC circuits are configured to couple to analogue signal receiving and adjusting circuits, receive and convert the adjusted analogue signals to digital signals (data);

wherein the flash memory is configured to be connected to the FPGA device and to store the FPGA programming code (intellectual Property, IP);

35 wherein clock generating circuits are configured to provide operating clock to the FPGA device and various digital circuits on the DAQ module;

wherein RAM is configured to be connected to the FPGA device and provide additional data memory;

40 wherein the power supply circuits are configured to provide power supplies of various voltages to the each circuit on the DAQ module, and in case necessary, 5V to the connected SBC.

45 11. According to claim 6, 8 to 10, wherein DAQ module further comprising:
FPGA IPs loaded in the flash memory on the DAQ module, which further comprising:

50 IP to control the operations of the aforesaid analogue signal receiving and adjusting circuits and ADC circuits,
IP to pick up digital signals from the aforesaid ADC and to process the digital signals (data),
IP to write data to and read data from the aforesaid RAM,

IP to perform data and instruction exchanges with the SBC via the aforesaid pin-to-pin connections of the IO and GPIO pins according to a specially stipulated communication protocol.

5 12. Claim 6 to 11, wherein a SBC further comprising:

Linux operating system,
software library functions, and
application programs,

10 wherein the software library functions are configure to implement a specially stipulated communication protocol for data and instruction exchanges with a DAQ module via the pin-to-pin connection of the aforesaid connectors,

15 wherein the application programs further comprising at least the following programs:

programs for exchanging data and commands between the SBC and the DAQ module by calling the aforesaid library functions,
programs to process data read from FPGA,
programs to perform other functionalities as required by the designed
20 apparatus.