CLAIMS

1. A method to fabricate a quantum computing device, the method comprising:

forming a first chip having a first substrate, a first set of pads, and a set of Josephson junctions disposed on the first substrate; and

forming a second chip having a second substrate, a second set of pads disposed on the second substrate opposite the first set of pads, and a second layer formed on a subset of the second set of pads, the second layer configured to bond the first chip and the second chip, wherein the subset of the second set of pads corresponds to a subset of the set of Josephson junctions selected to avoid frequency collision between qubits in a set of qubits, a qubit in the set of qubits resulting from a Josephson junction in the subset of Josephson junctions.

2. The method of claim 1, further comprising:

forming an unusable Josephson junction in the set of Josephson junctions, wherein a first Josephson junction in the set of Josephson junctions is modified to become the unusable Josephson junction responsive to the first Josephson junction being excluded from the subset of the set of Josephson junctions.

3. The method of claim 2, further comprising:

forming a disconnected pad in the first set of pads, wherein the first set of pads comprises a first pad electrically coupled to the first Josephson junction, and wherein the first pad is electrically disconnected from the first Josephson junction to form the disconnected pad, the disconnected pad rendering the first Josephson junction unusable.

4. The method of claim 2, wherein an electrical property of the first Josephson junction is modified such that the first Josephson junction no longer operates as a Josephson junction.

5. The method of any of the preceding claims, wherein the subset is selected based upon a measurement of a parameter associated with each of the set of Josephson junctions.

6. The method of claim 5, wherein the resonance frequency associated with a particular qubit is one member selected from a set of (i) a predicted resonance frequency calculated based upon the measured parameter, and (ii) an actual measured resonance frequency of the particular qubit.

7. The method of claim 5, wherein the parameter includes a resistance associated with a Josephson junction in the set of Josephson junctions.

8. The method of claim 7, wherein the resistance is a normal-state resistance of the Josephson junction.

9. The method of any of the preceding claims, further comprising:

forming a first set of protrusions formed on the first chip; and

forming a set of bumps formed on the first layer of the second chip, the set of bumps formed of a material having above a threshold ductility at a room temperature range, wherein set of bumps are configured to cold weld to the first set of protrusions.

10. The method of claim 9, wherein the first set of protrusions is of at least one member selected from a set comprising Gold and Platinum.

11. The method of either claim 9 or 10, wherein the set of bumps is of at least one member selected from a set comprising Indium, Tin, Lead, and Bismuth.

12. The method of any of claims 9 to 11, further comprising:

forming a flip-chip assembly comprising the first chip detachably attached to the second chip using the cold weld, wherein a parameter of a Josephson junction inside the flip-chip assembly is tunable by disassembling the flip-chip assembly at the cold weld.

13. A superconductor fabrication system comprising a lithography component, the superconductor fabrication system when operated on at least one die to fabricate a quantum computing device for performing the method of any of claims 1 to 12.

14. A method to fabricate a quantum processor, the method comprising:

forming a set of qubits, at least one qubit in the set of qubits formed in a flip-chip configuration comprising a pair of chips, forming the pair of chips comprising:

forming a first chip having a first substrate, a first set of pads, and a set of Josephson junctions disposed on the first substrate; and

forming a second chip having a second substrate, a second set of pads disposed on the second substrate opposite the first set of pads, and a second layer formed on a subset of the second set of pads, the second layer configured to bond the first chip and the second chip, wherein the subset of the second set of pads corresponds to a subset of the set of Josephson junctions selected to avoid frequency collision between qubits in the set of qubits, a qubit in the set of qubits resulting from a Josephson junction in the subset of Josephson junctions.