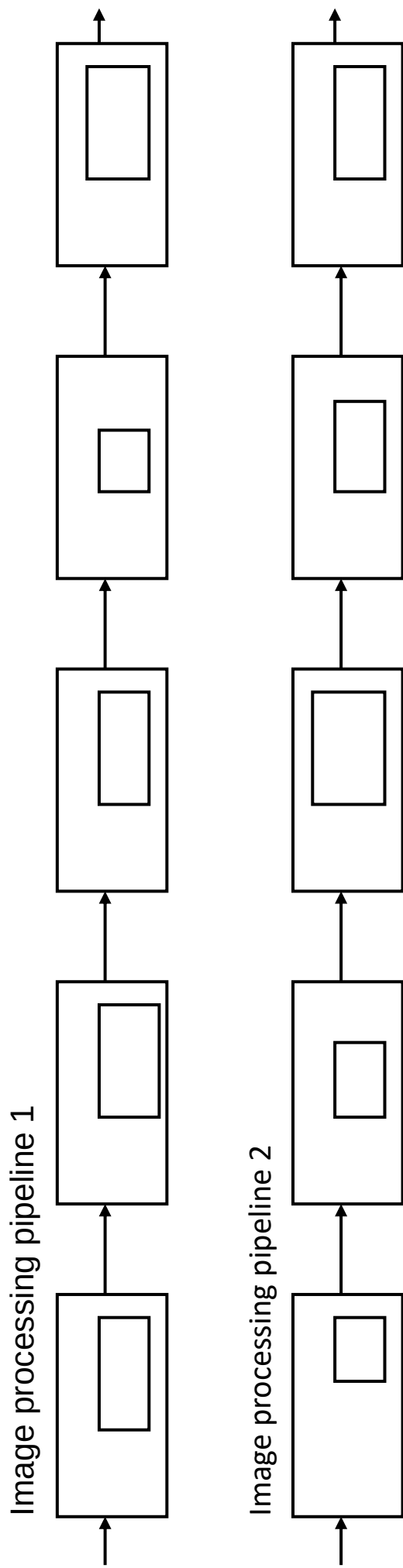


# Image Processing Pipelines



- Image processing blocks with internal memory
- Multiple pipelines used one at a time
- Waste of memory

Figure 1

## Centralise memory and share through fabric

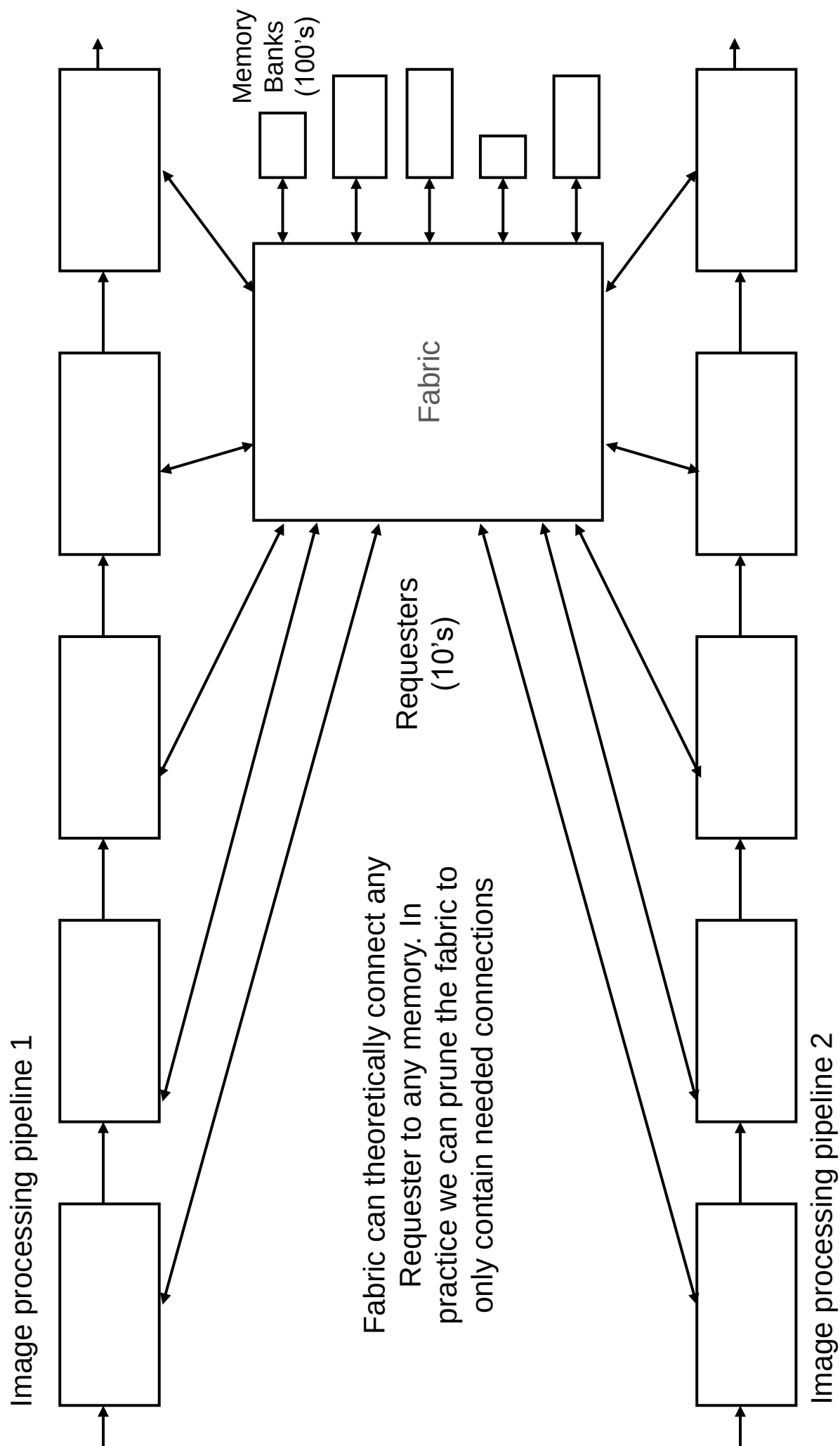


Figure 2

Example connections

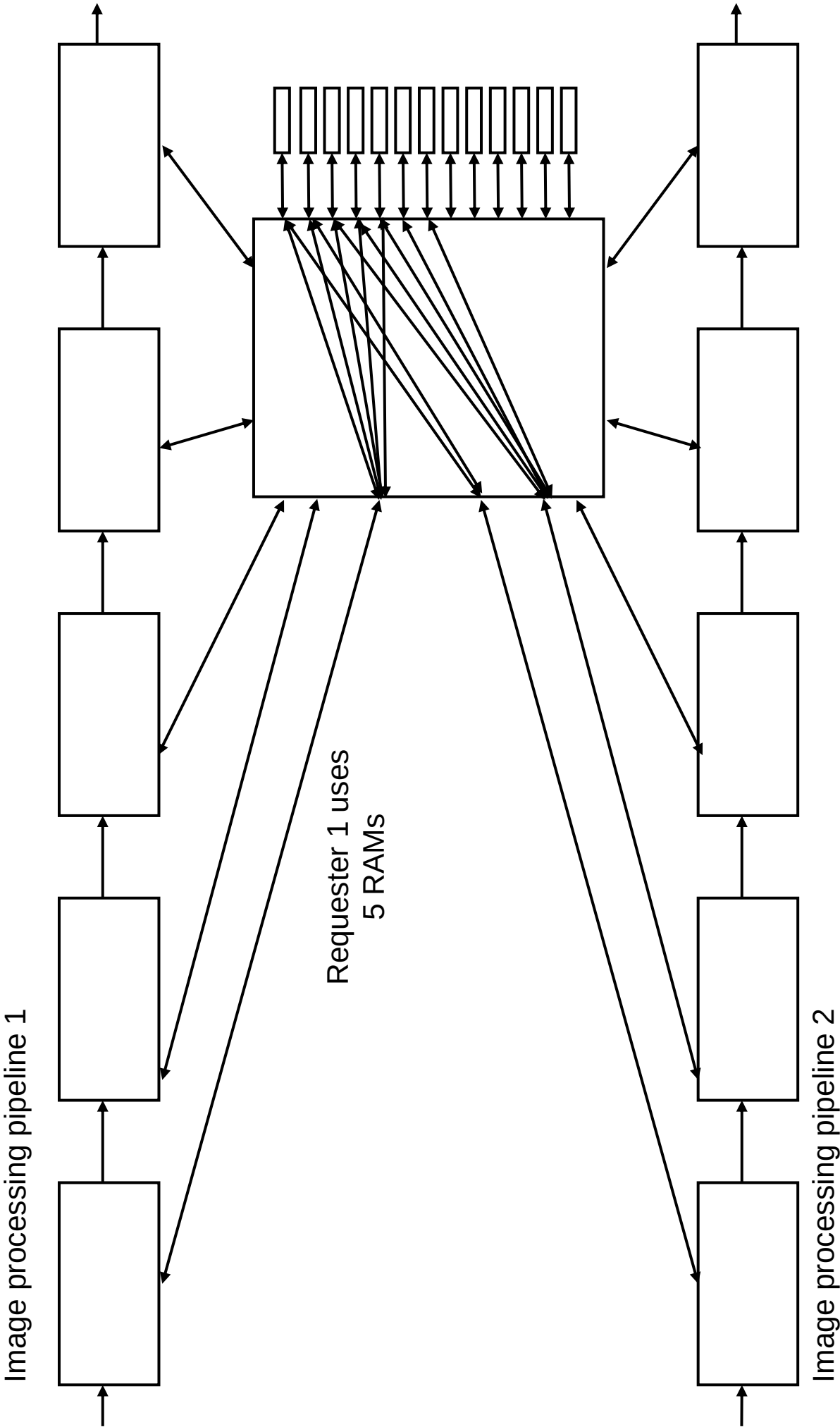


Figure 3

# Example active connections

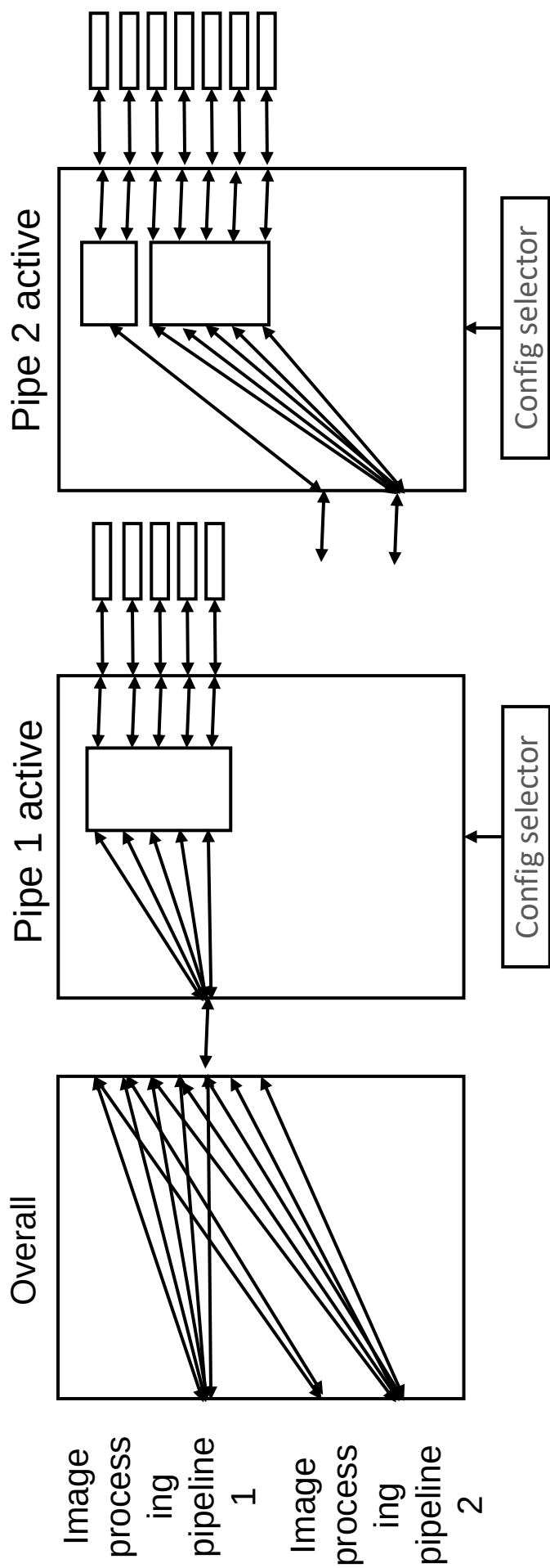
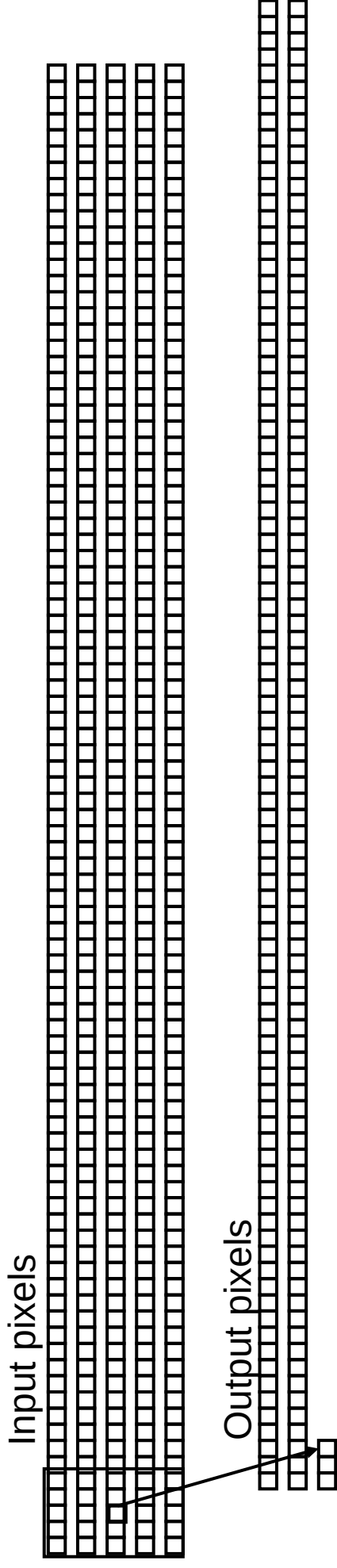


Figure 4

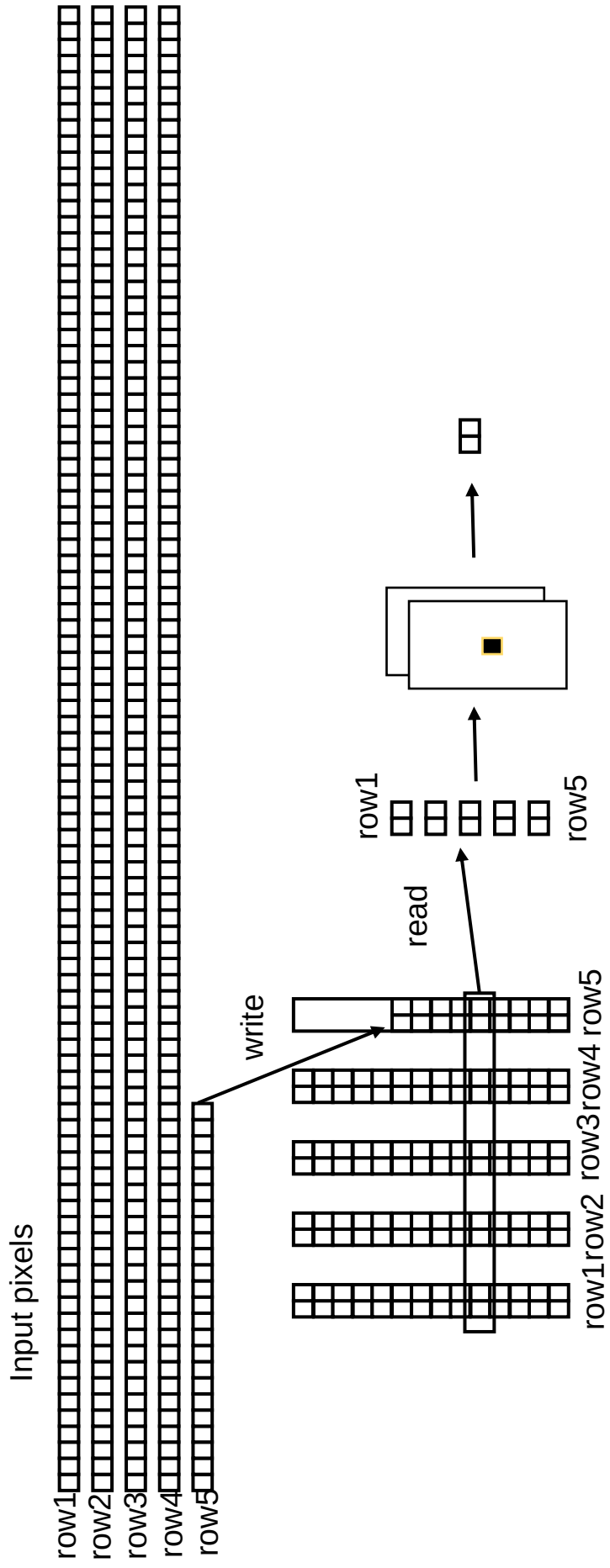
# Example Image Processing block



- Pixels arrive in sequentially in rows
- Use 5x5 input pixels to calculate each output pixel

Figure 5

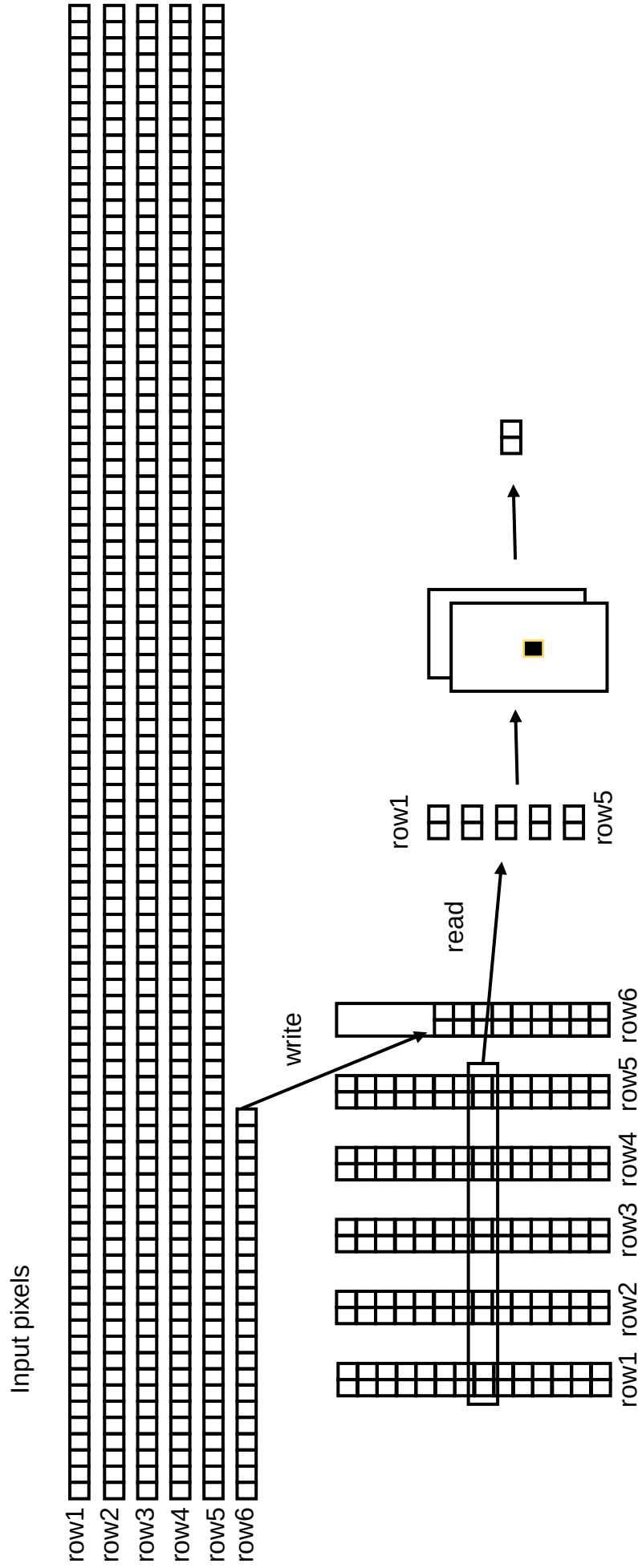
# Example memory write/read pattern



- Write pixels in pairs, one memory for each row
- When 5 rows have been stored can start reading all five memories and load into buffer to do 5x5 calculation
- Reads of 2 pixels from each row -> 2 output pixels calculated

Figure 6

# Dual port emulation



- Extra RAM so don't need to read and write to same memory in one cycle

Figure 7

# Requester 1 Write path

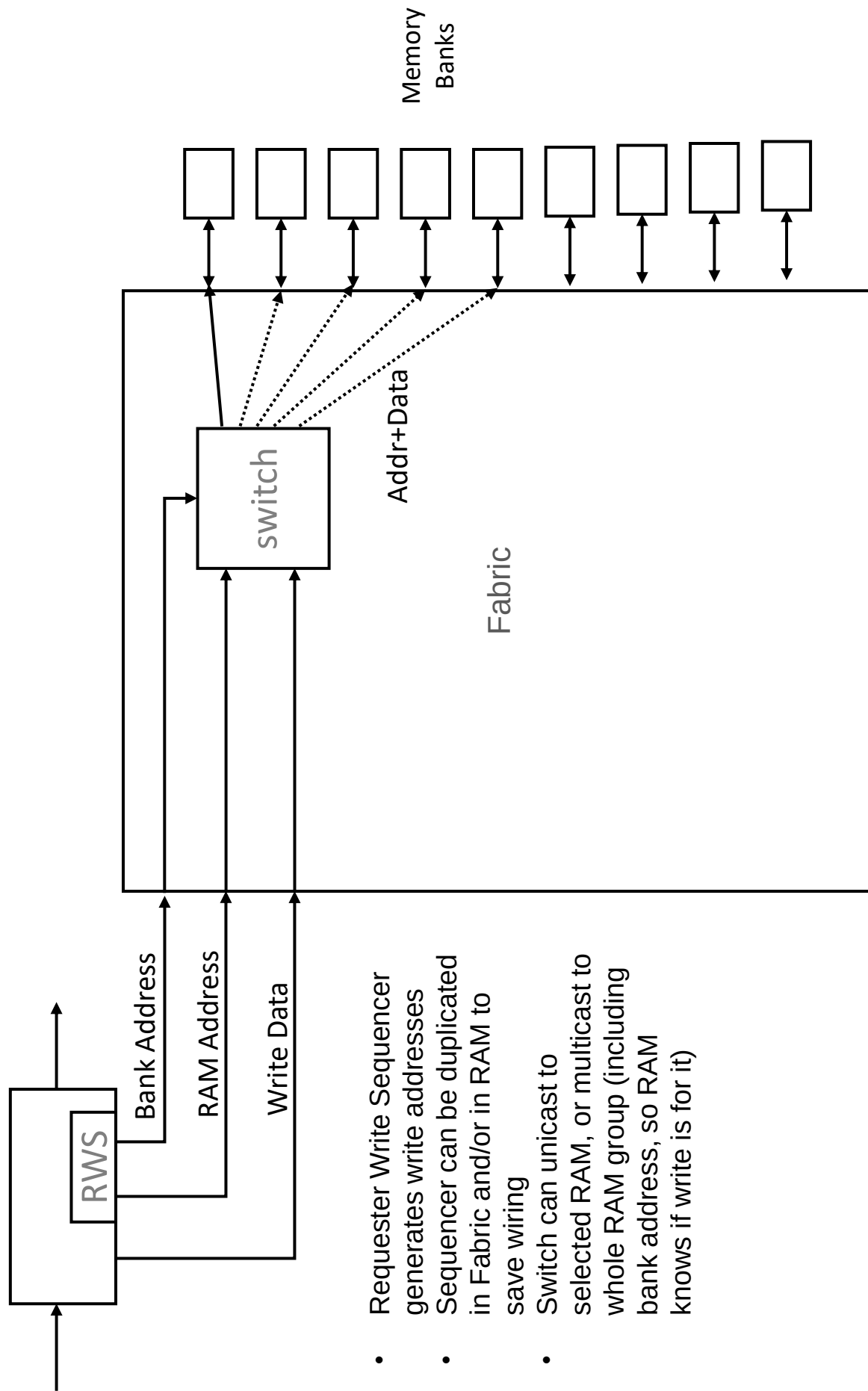


Figure 8

# Requester 1 Read path

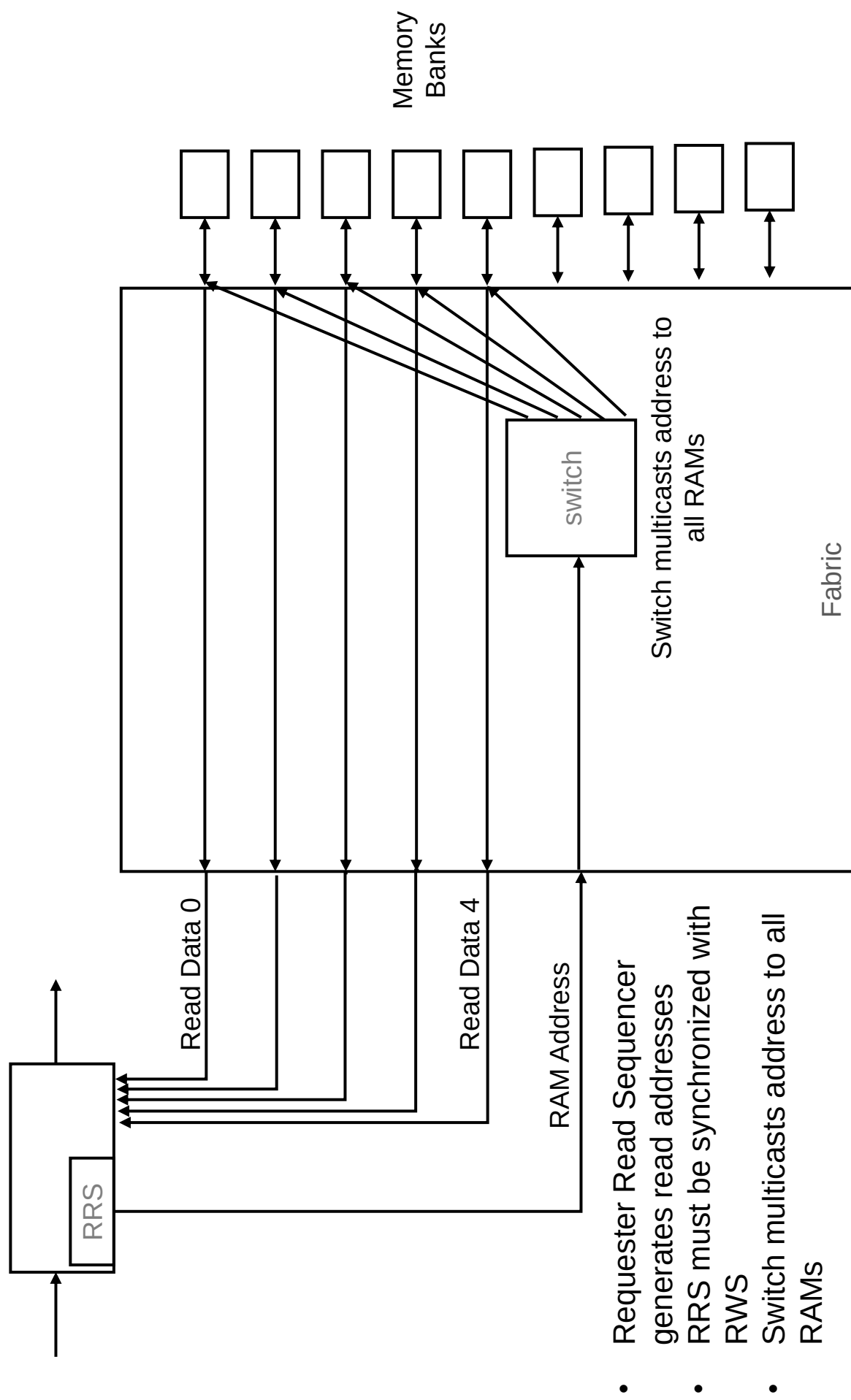


Figure 9

# Requester 1 Read path dual port emulation

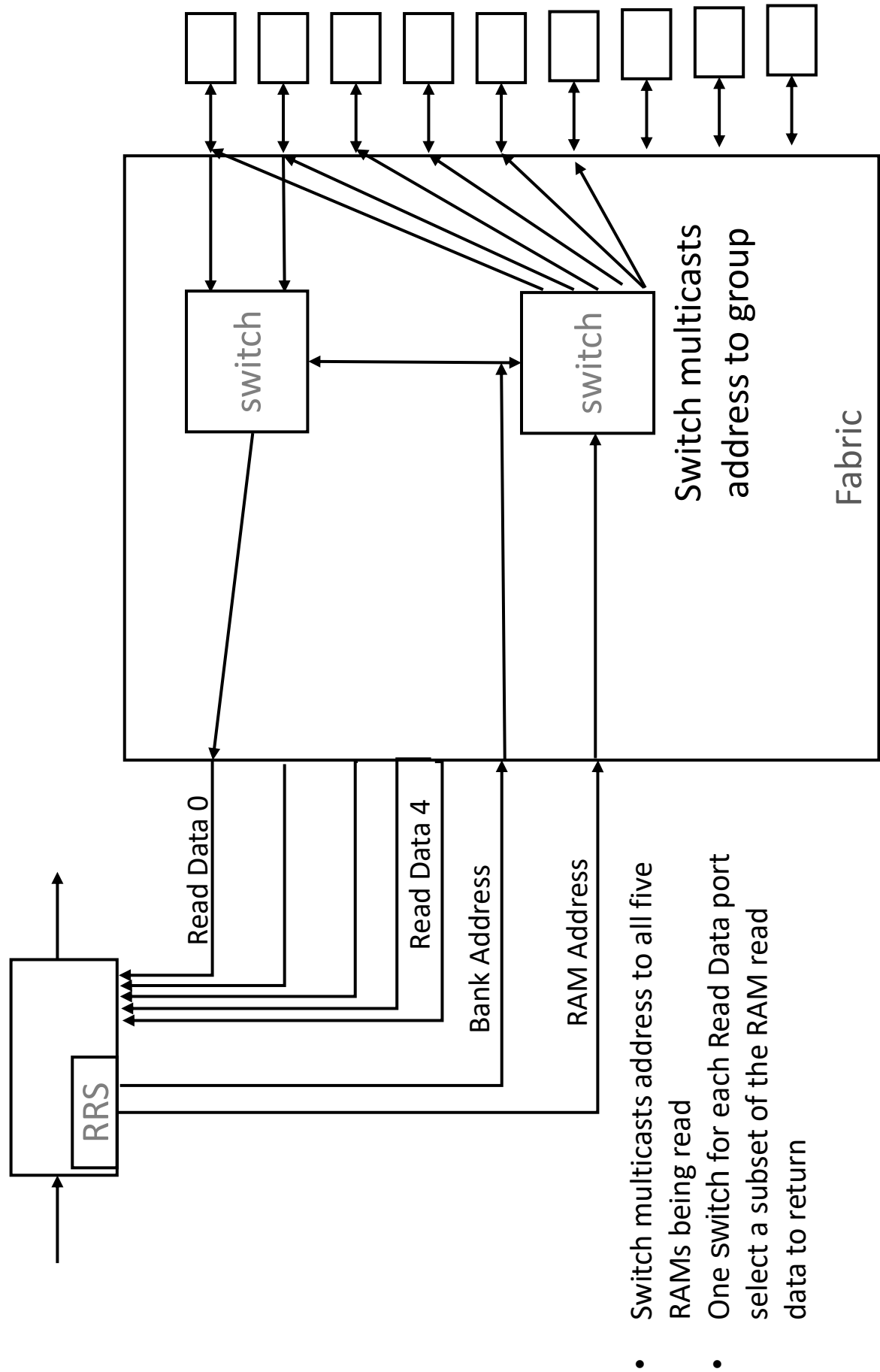
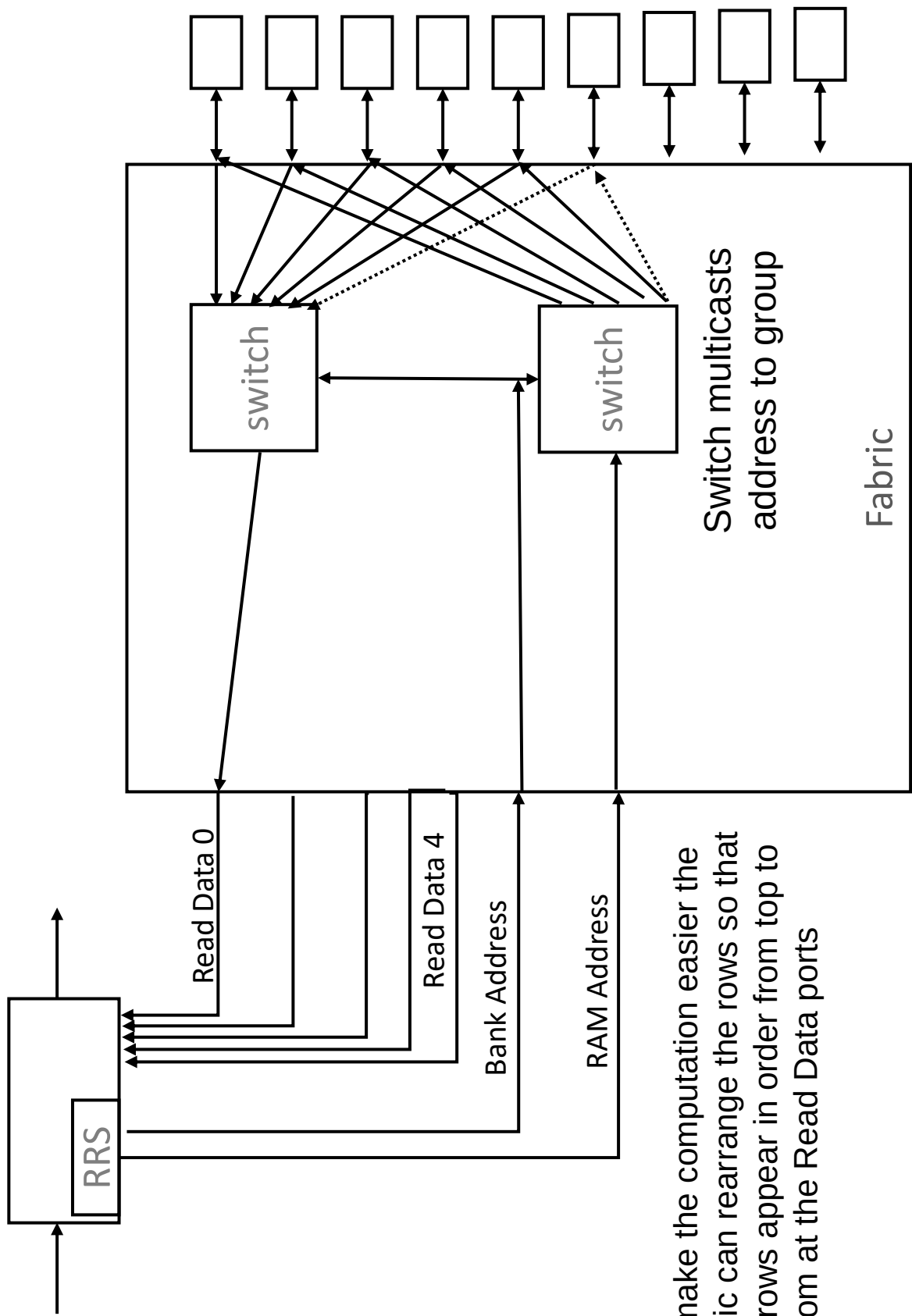


Figure 10

Requester 1 Read path row rearrangement



- To make the computation easier the fabric can rearrange the rows so that the rows appear in order from top to bottom at the Read Data ports

Figure 11

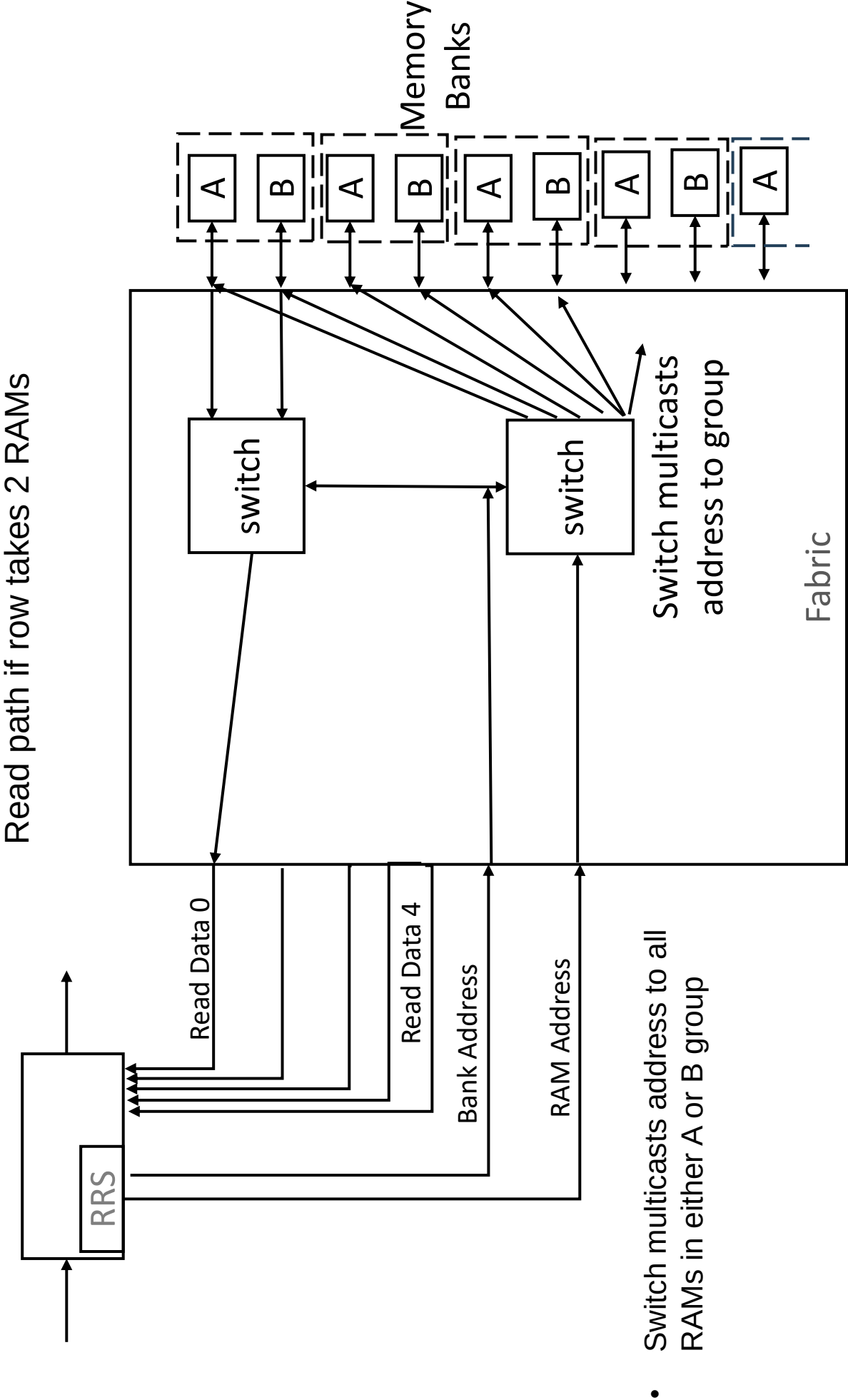


Figure 12

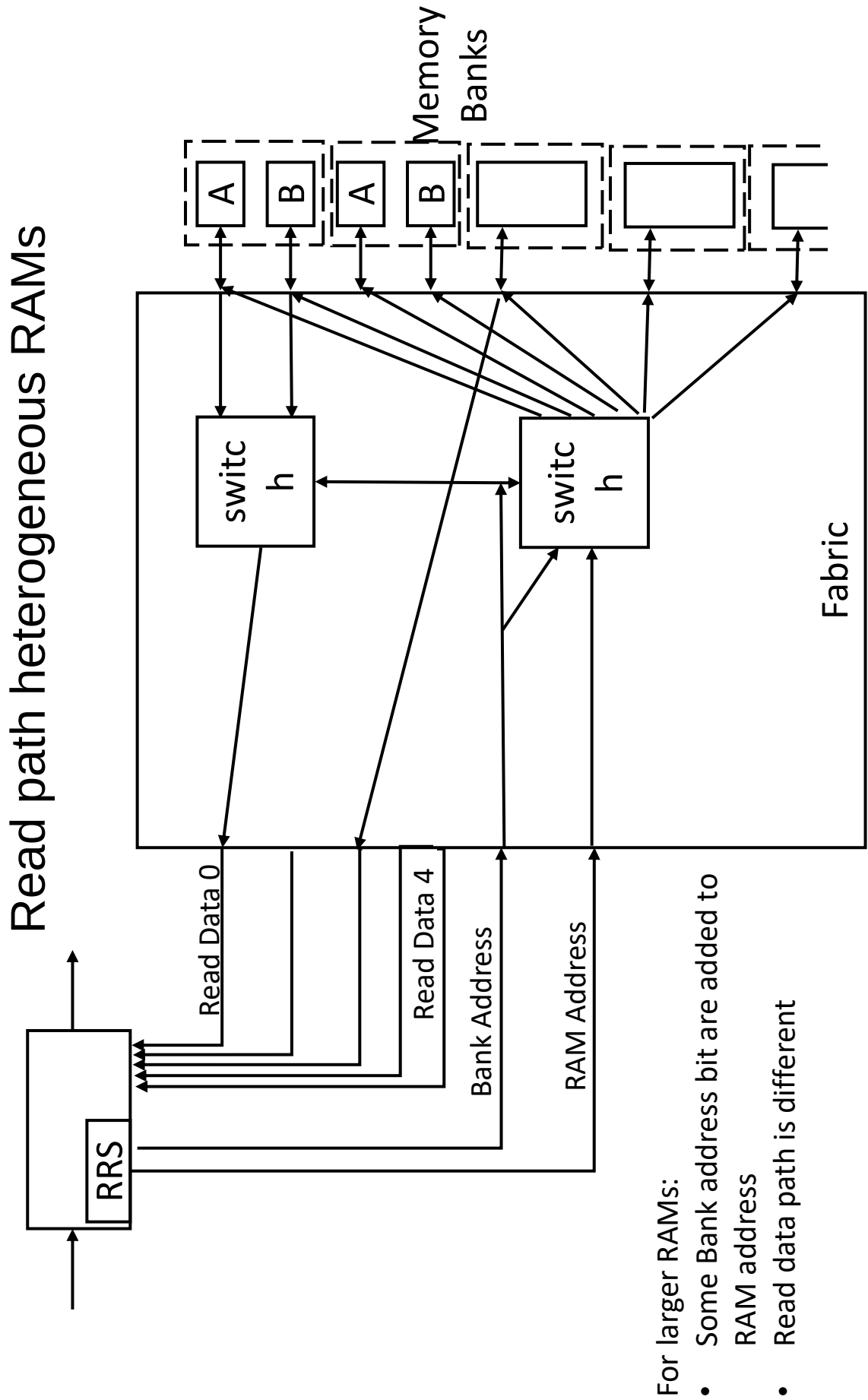
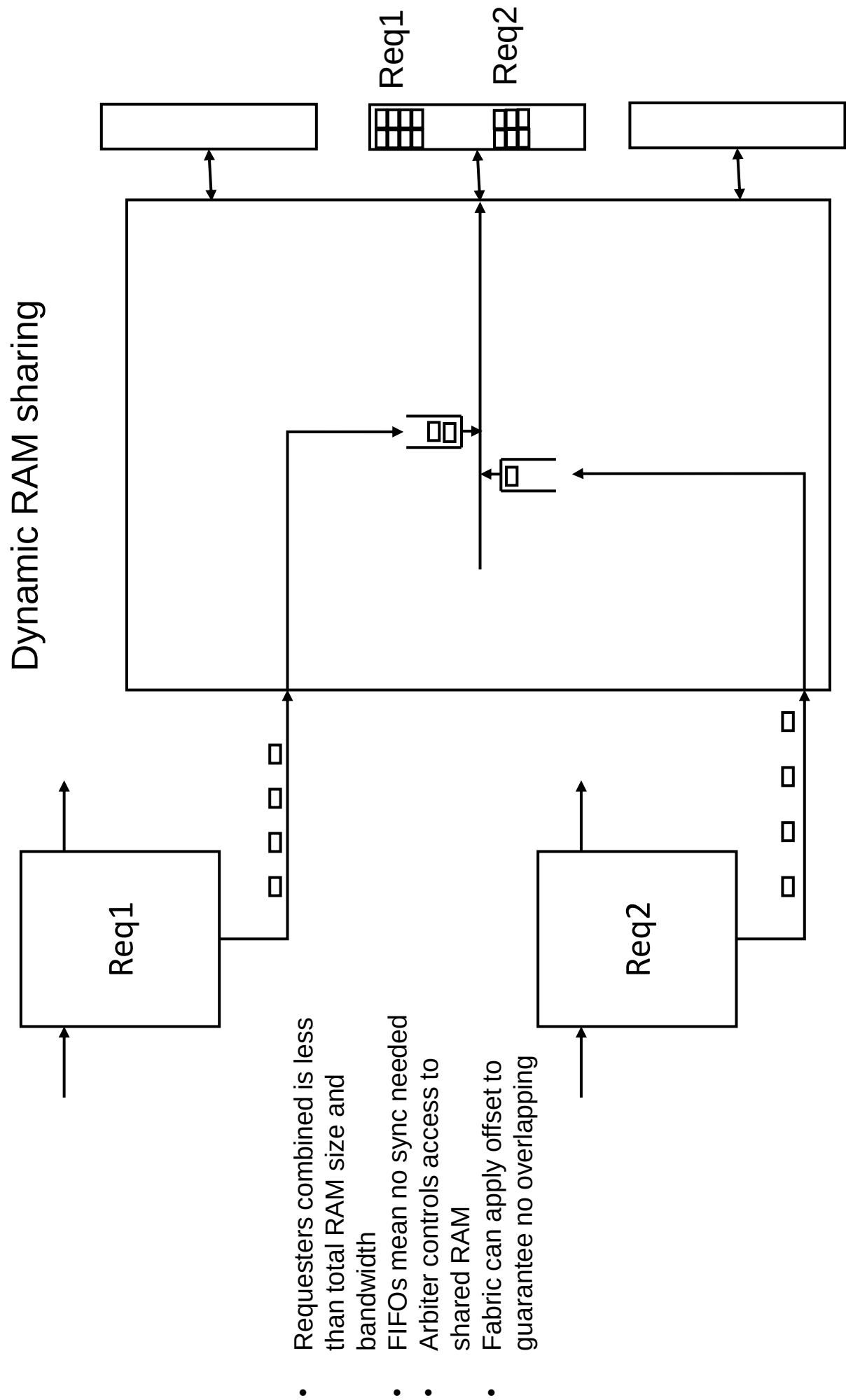


Figure 13



- Requesters combined is less than total RAM size and bandwidth
- FIFOs mean no sync needed
- Arbiter controls access to shared RAM
- Fabric can apply offset to guarantee no overlapping

Figure 14

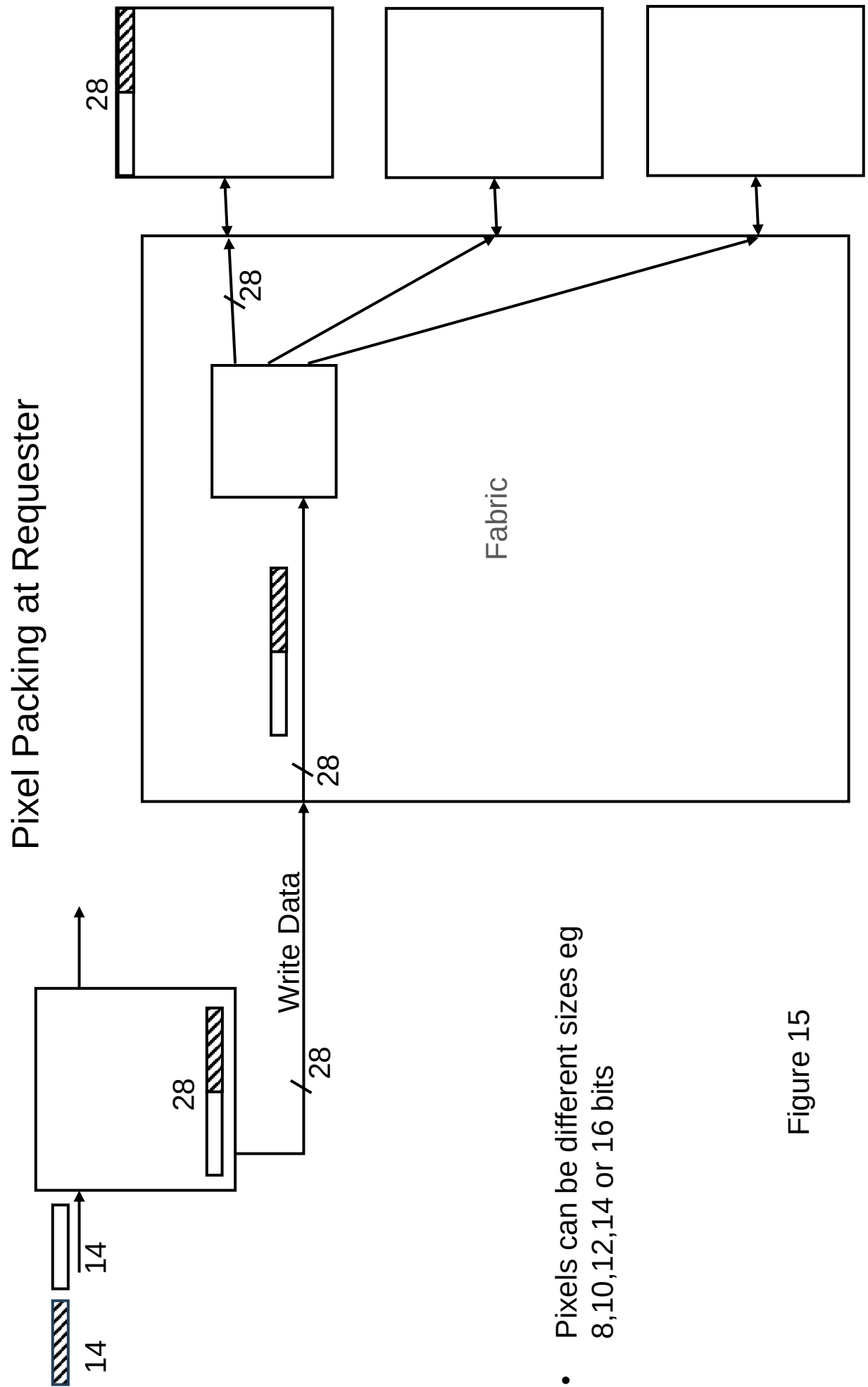
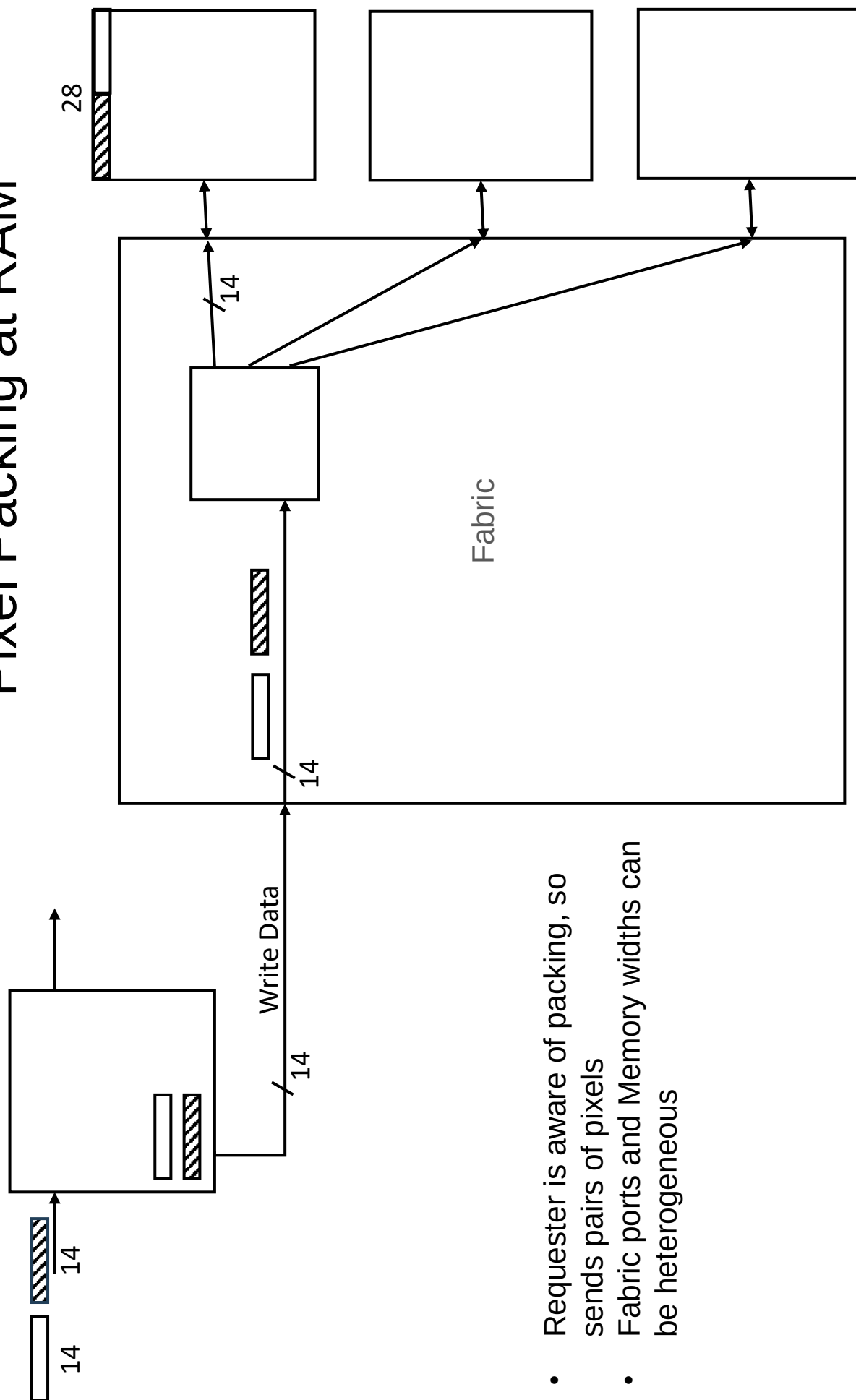


Figure 15

# Pixel Packing at RAM



- Requester is aware of packing, so sends pairs of pixels
- Fabric ports and Memory widths can be heterogeneous

Figure 16

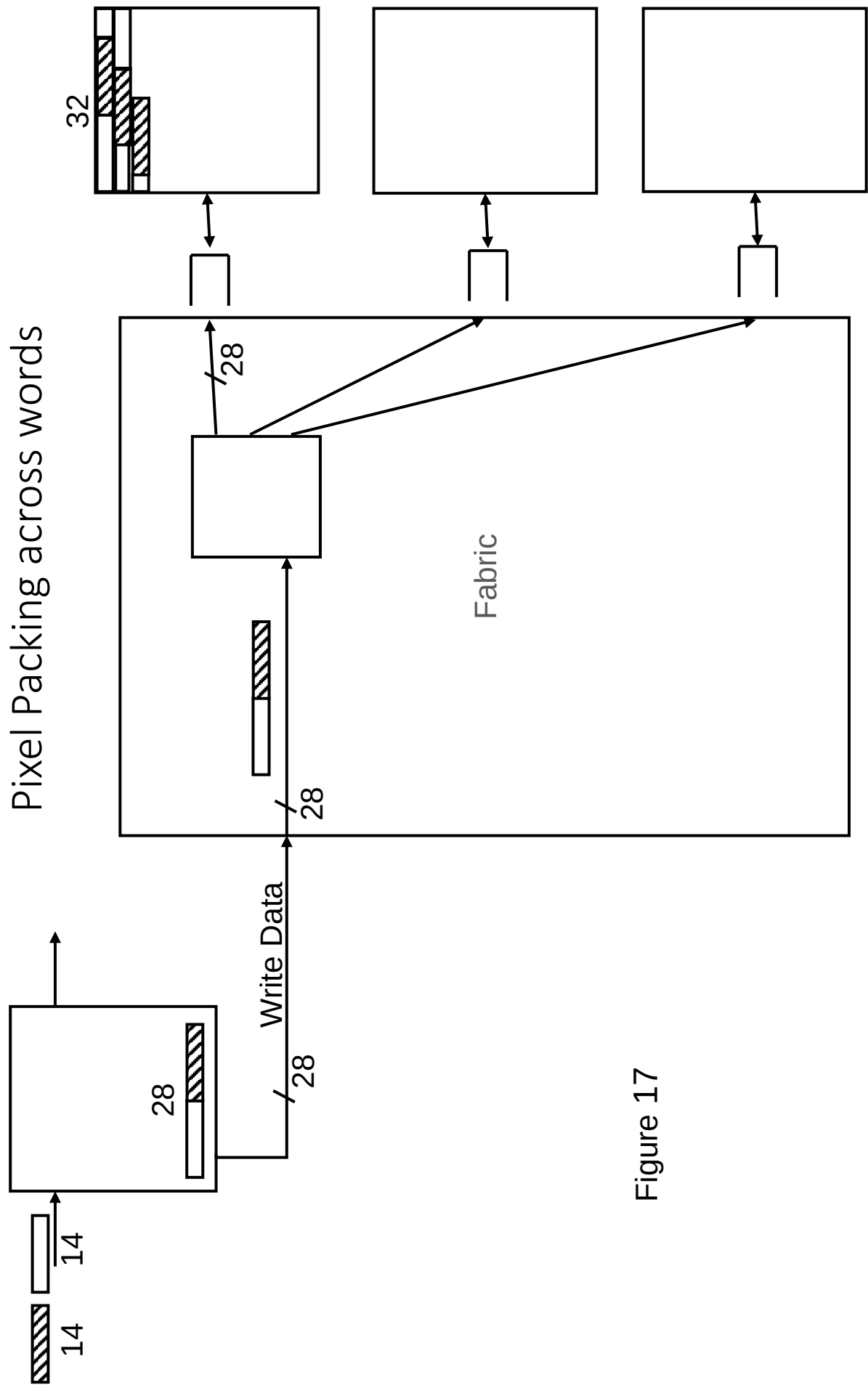


Figure 17

Switch Fabrics

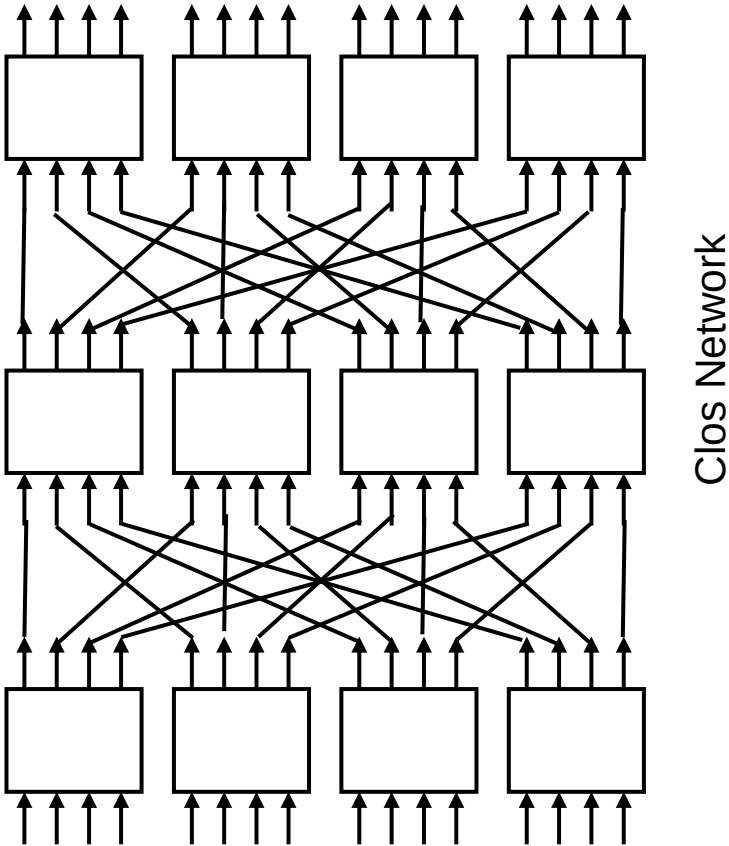
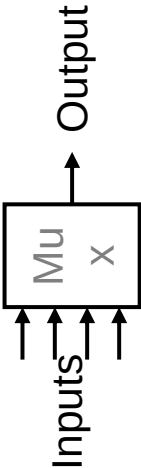
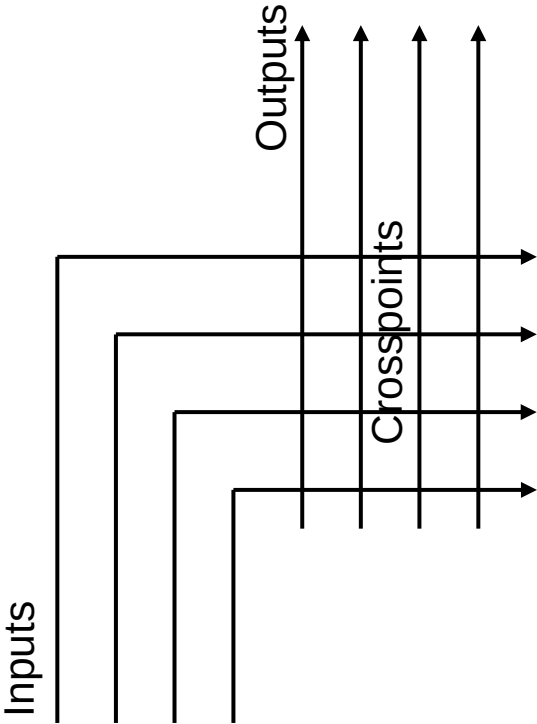


Figure 18

## Other accesses

- RAMs may act as a lookup tables, data needs to be written by CPU (only useful if lookup shared)
- Read access may be needed for debugging (also possibly write)
- Self test units (BIST) may access RAMs across the fabric

Figure 19

Multistage fabric for efficient layout

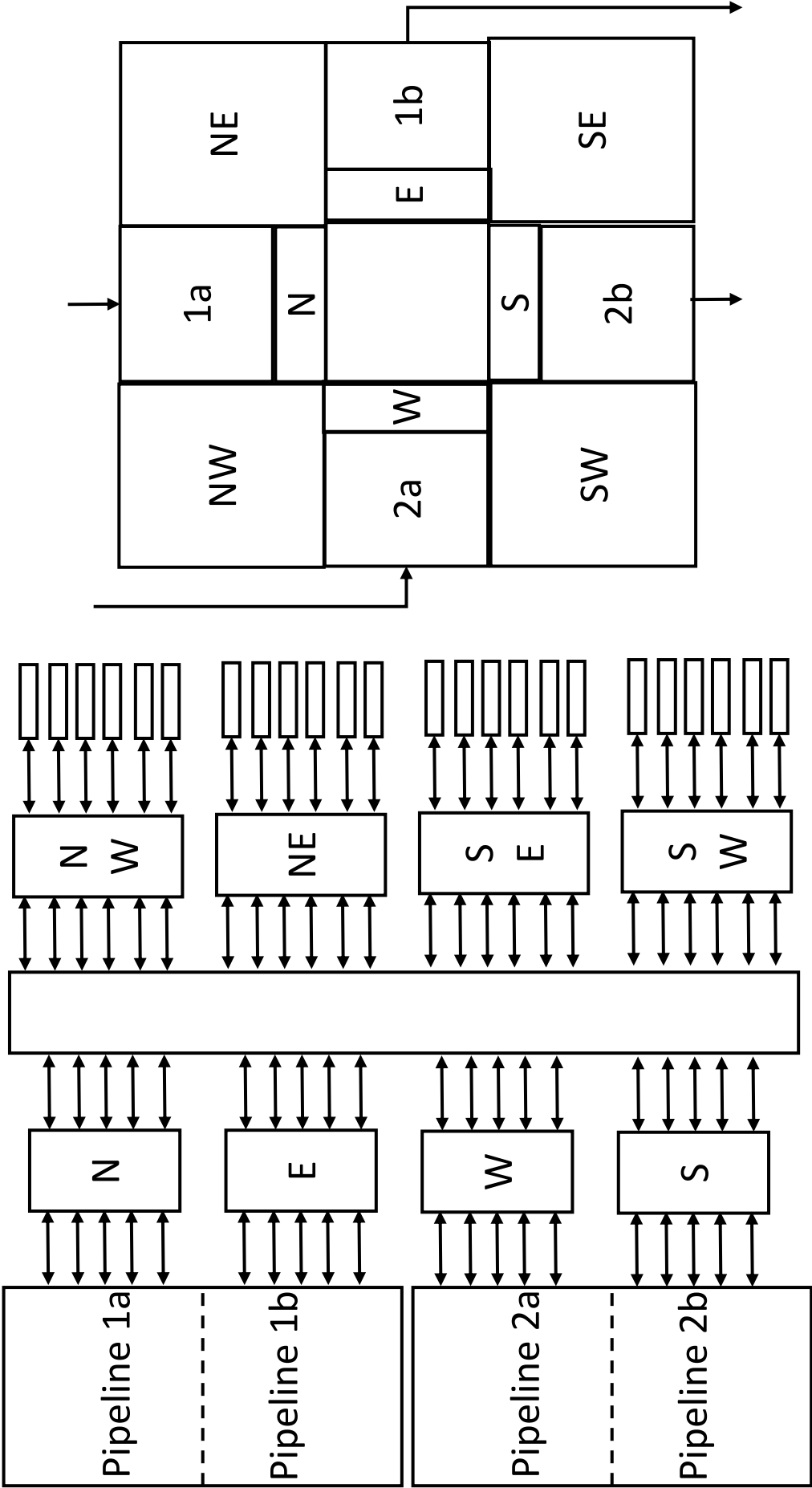


Figure 20