WHAT IS CLAIMED IS:

1. An integrated circuit semiconductor device comprising:

a plurality of cylindrical structures separated from each other on a substrate; and

a plurality of supporters having an opening region exposing side surfaces of the plurality of cylindrical structures, the plurality of supporters being in contact with the side surfaces of the plurality of cylindrical structures and supporting the plurality of cylindrical structures,

wherein each of the plurality of supporters has side surfaces being in contact with the side surfaces of the plurality of cylindrical structures and having slopes, and has a top width that is less than a bottom width, and

wherein each of the plurality of cylindrical structures higher than the plurality of supporters has side surfaces, on which a dielectric layer and an upper electrode are formed, having slopes and has a top width that is less than a bottom width.

2. The integrated circuit semiconductor device of claim 1, wherein the plurality of supporters are at a height that is lower than top surfaces of the plurality of cylindrical structures.

3. The integrated circuit semiconductor device of claim 1 or claim 2, wherein a top space between the plurality of cylindrical structures higher than the plurality of supporters is greater than a bottom space therebetween.

4. The integrated circuit semiconductor device of any one of claims 1 to 3, wherein each of the plurality of cylindrical structures at the same level as the plurality of supporters has side surfaces being in contact with the side surfaces of the plurality of supporters and having slopes, and has a top width that is greater than a bottom width.

5. The integrated circuit semiconductor device of any one of claims 1 to 4, wherein each of the plurality of cylindrical structures lower than the plurality of supporters has side surfaces, on which the dielectric layer and the upper electrode are formed, having slopes and has a top width that is greater than a bottom width.

6. The integrated circuit semiconductor device of any one of claims 1 to 5, further comprising additional supporters below the plurality of supporters, the additional supporters being in contact with the side surfaces of the plurality of cylindrical structures and supporting the plurality of cylindrical structures.

7. The integrated circuit semiconductor device of claim 1, wherein the plurality of supporters are at a height that is lower than top surfaces of the plurality of cylindrical structures, and

each of the plurality of cylindrical structures higher than the plurality of supporters has the side surfaces recessed inward.

8. The integrated circuit semiconductor device of claim 1, wherein the plurality of supporters are at a height that is lower than top surfaces of the plurality of cylindrical structures, and

each of the plurality of cylindrical structures lower than the plurality of supporters has side surfaces, on which the dielectric layer and the upper electrode are formed, having slopes and recessed inward and has a top width that is greater than a bottom width.

9. The integrated circuit semiconductor device of any one of claims 1 to 8, wherein the plurality of cylindrical structures include cylindrical lower electrodes having a seam therein, the dielectric layer is between the cylindrical lower electrodes and on side surfaces of the cylindrical lower electrodes, and the upper electrode is on the dielectric layer.

10. An integrated circuit semiconductor device comprising:

a plurality of cylindrical structures separated from each other on a substrate; and

a plurality of supporters having an opening region exposing side surfaces of the plurality of cylindrical structures, the plurality of supporters being in contact with the side surfaces of the plurality of cylindrical structures, being at a height that is lower than top surfaces of the plurality of cylindrical structures, and supporting the plurality of cylindrical structures,

wherein the plurality of cylindrical structures include a first level electrode portion, a second level electrode portion, and a third level electrode portion, the first level electrode portion having a first height from the substrate, the second level electrode portion having a

second height from a top of the first level electrode portion, and the third level electrode portion having a third height from a top of the second level electrode portion,

the first level electrode portion has side surfaces, on which a dielectric layer and an upper electrode are formed, having slopes, the second level electrode portion has side surfaces being in contact with side surfaces of the plurality of supporters and having slopes, each of the first level electrode portion and the second level electrode portion has a top width that is greater than a bottom width, and the third level electrode portion has side surfaces, on which the dielectric layer and the upper electrode are formed, having slopes and has a top width that is less than a bottom width, and

a side surface of the first level electrode portion and a side surface of the second level electrode portion are connected to a side surface of the third level electrode portion, and a slope of the side surfaces of the first and second level electrode portions is opposite a slope of the side surface of the third level electrode portion in positive and negative perspectives.

11. The integrated circuit semiconductor device of claim 10, wherein each of the plurality of supporters is at the side surface of the second level electrode portion.

12. The integrated circuit semiconductor device of claim 10 or claim 11, wherein each of the plurality of supporters has the side surfaces being in contact with the side surfaces of the plurality of cylindrical structures and having slopes, and has a top width that is less than a bottom width.

13. The integrated circuit semiconductor device of any one of claims 10 to 12, wherein the first height of the first level electrode portion is greater than the second height of the second level electrode portion and the third height of the third level electrode portion, and

additional supporters are formed in a side wall of the first level electrode portion.

14. The integrated circuit semiconductor device of any one of claims 11 to 13, wherein the first level electrode portion includes a lower level electrode portion on a top of the substrate and an upper level electrode portion on the lower level electrode portion,

side walls of each of the plurality of cylindrical structures between the lower level

electrode portion and the upper level electrode portion, on which the dielectric layer and the upper electrode are formed, have slopes, and

a bottom width of the upper level electrode portion is less than a top width of the lower level electrode portion.

15. The integrated circuit semiconductor device of any one of claims 10 to 13, wherein the first level electrode portion includes a lower level electrode portion on a top of the substrate and an upper level electrode portion on the lower level electrode portion, and

the bottom width of the second level electrode portion is greater than a top width of the upper level electrode portion.

16. The integrated circuit semiconductor device of any one of claims 10 to 15, wherein the bottom width of the third level electrode portion is less than the top width of the second level electrode portion.

17. An integrated circuit semiconductor device comprising:

a plurality of cylindrical structures separated from each other on a substrate; and

a plurality of supporters having an opening region exposing side surfaces of the plurality of cylindrical structures, the plurality of supporters being in contact with the side surfaces of the plurality of cylindrical structures and supporting the plurality of cylindrical structures,

wherein the plurality of cylindrical structures include a first level electrode portion, a second level electrode portion, and a third level electrode portion, the first level electrode portion having a first height from the substrate, the second level electrode portion having a second height from a top of the first level electrode portion, and the third level electrode portion having a third height from a top of the second level electrode portion,

the first level electrode portion has side surfaces, on which a dielectric layer and an upper electrode are formed, having slopes, the second level electrode portion has side surfaces being in contact with side surfaces of the plurality of supporters and having slopes, each of the first level electrode portion and the second level electrode portion has a top width that is greater than a bottom width, and the third level electrode portion has side surfaces, on which the dielectric layer and the upper electrode are formed, having slopes and has a top width that is less than a bottom width,

in a cross-sectional view of the integrated circuit semiconductor device, a side surface and an opposite side surface, on which the dielectric layer and the upper electrode are formed, of the first level electrode portion respectively have a positive slope and a negative slope, a side surface and an opposite side surface, in contact with the side surfaces of the plurality of supporters, of the second level electrode portion respectively have a positive slope and a negative slope, a side surface, on which the dielectric layer and the upper electrode are formed, of the third level electrode portion connected to the side surfaces of each of the first and second level electrode portions has a negative slope, and an opposite side surface, on which the dielectric layer and the upper electrode are formed, of the third level electrode portion connected to the opposite side surfaces of each of the first and second level electrode portions has a positive slope, and

each of the plurality of supporters is at the side surface of the second level electrode portion, has the side surfaces being in contact with the side surface of the second level electrode portion and having slopes, and has a top width that is less than a bottom width.

18. The integrated circuit semiconductor device of claim 17, wherein the first level electrode portion includes a lower level electrode portion on a top of the substrate and an upper level electrode portion on the lower level electrode portion,

the upper level electrode portion is recessed inward and has a bottom width that is less than a top width of the lower level electrode portion,

side walls of each of the plurality of cylindrical structures between the lower level electrode portion and the upper level electrode portion, on which the dielectric layer and the upper electrode are formed, have slopes, and

the bottom width of the second level electrode portion is greater than a top width of the upper level electrode portion.

19. The integrated circuit semiconductor device of claim 17 or claim 18, wherein the third level electrode portion is recessed inward, and the bottom width of the third level electrode portion is less than the top width of the second level electrode portion.