CLAIMS

What is claimed is:

1. A method of forming a microelectronic device, comprising:

forming a microelectronic device structure, the microelectronic device structure comprising:

a stack structure comprising insulative structures and additional insulative structures vertically alternating with the insulative structures;

a dielectric structure vertically extending partially through the stack structure; and

a dielectric material vertically overlying and horizontally extending across the stack structure and the dielectric structure;

removing portions of the dielectric material, the dielectric structure, and the stack structure horizontally neighboring the dielectric structure to form a trench vertically overlying and at least partially horizontally overlapping a remaining portion of the dielectric structure; and

substantially filling the trench with additional dielectric material to form a dielectric-filled trench comprising a lower portion and an upper portion having a greater horizontal width than the lower portion.

2. The method of claim 1, wherein removing portions of the dielectric material and the dielectric structure to form a trench comprises forming the trench to divide the dielectric material into two sections discontinuous with one another.

3. The method of claim 1, wherein removing portions of the dielectric material and the dielectric structure to form a trench further comprises removing portions of the stack structure horizontally neighboring the dielectric structure.

4. The method of claim 1, further comprising:

forming contact openings vertically extending completely through the dielectric material and the stack structure; and

forming contact structures within the contact openings.

5. The method of claim 4, further comprising replacing the dielectric material and the additional insulative structures of the stack structure with electrically conductive material after forming the contact structures within the contact openings.

6. The method of one of claims 4 and 5, wherein substantially filling the trench with additional dielectric material comprises filling the trench with the additional dielectric material prior to forming the contact openings.

7. The method of claim 6, further comprising:

horizontally recessing portions of the dielectric material and the additional insulative structures adjacent the contact openings relative to portions of the insulative structures adjacent the contact openings to form enlarged contact openings having non-planar horizontal boundaries;

forming dielectric liner structures within the enlarged contact openings; and

filling remaining portions of the enlarged contact openings with electrically conductive material to form the contact structures, the dielectric liner structures horizontally intervening between the contact structures and the stack structure.

8. The method of one of claims 4 and 5, wherein substantially filling the trench with additional dielectric material comprises filling trench with the additional dielectric material after forming the contact openings.

9. The method of claim 8, further comprising:

forming a masking structure over the dielectric material after forming the trench, the masking structure covering the trench without substantially vertically extending into the trench;

forming the contact openings using the masking structure;

removing portions of the masking structure remaining after forming the contact openings to expose the trench;

enlarging horizontal dimensions of the contact openings and the trench;

forming the additional dielectric material within the contact openings and the trench after enlarging the horizontal dimensions thereof, the additional dielectric material partially filling the contact openings and substantially filling the trench;

removing portions of the additional dielectric material at bottoms of the contact openings to form dielectric liner structures within the contact openings; and

filling remaining portions of the contact openings with electrically conductive material to form the contact structures, the dielectric liner structures horizontally intervening between the contact structures and the stack structure.

10. The method of claim 9, wherein enlarging horizontal dimensions of the contact openings and the trench comprises horizontally recessing portions of the dielectric material and the additional insulative structures adjacent the contact openings and the trench relative to portions of the insulative structures adjacent the contact openings and the trench.

11. The method of one of claims 4 and 5, further comprising forming at least some of the contact structures to individually physically contact discrete conductive structures vertically underlying the stack structure.

12. The method of claim 11, wherein forming at least some of the contact structures to individually physically contact discrete conductive structures vertically underlying the stack structure comprises offsetting horizontal centers of the at least some of the contact structures from horizontal centers of the discrete conductive structures in physical contact therewith.

13. The method of one of claims 4 and 5, wherein forming contact structures within the contact openings comprises forming at least some of the contact structures to have oblong horizontal cross-sectional shapes.

14. A microelectronic device, comprising:

a stack structure comprising vertically alternating conductive structures and insulating structures arranged in tiers, each of the tiers comprising one of the conductive structures and one of the insulating structures;

a filled trench partially vertically extending through the stack structure and horizontally extending in a first direction, the filled trench comprising:

a lower portion; and

an upper portion having a greater horizontal width in a second direction orthogonal to the first direction than the lower portion; and

at least one dielectric structure within the filled trench.

15. The microelectronic device of claim 14, wherein horizontal boundaries of the upper portion of the filled trench are substantially non-planar.

16. The microelectronic device of claim 14, wherein horizontal boundaries of the upper portion of the filled trench are substantially planar.

17. The microelectronic device of any one of claims 14 through 16, further comprising:

a source tier underlying the stack structure and comprising:

a conductive source structure; and

discrete conductive structures horizontally separated from one another and the conductive source structure;

contact structures vertically extending completely through the stack structure to the discrete conductive structures of the source tier; and

dielectric liner structures horizontally intervening between the contact structures and the stack structure.

18. The microelectronic device of claim 17, wherein:

the contact structures have ovular horizontal cross-sectional shapes; and

horizontal centers of at least some of the contact structures are offset from horizontal centers of at least some of the discrete conductive structures physically contacting the at least some of the contact structures.

19. The microelectronic device of claim 17, further comprising:

a staircase structure having steps comprising edges of at least some of the tiers of the stack structure; and

additional contact structures on the steps of the staircase structure and horizontally alternating with at least some of the contact structures in the first direction.

20. A memory device, comprising:

a stack structure comprising tiers each comprising at least one conductive structure and at least one insulating structure vertically adjacent the at least one conductive structure;

dielectric-filled trenches partially vertically extending through the stack structure and each comprising:

a lower portion; and

an upper portion having one or more greater horizontal widths than the lower portion;

a staircase structure having steps comprising edges of the tiers of the stack structure;

a source tier underlying the stack structure and comprising:

a source plate; and

discrete conductive structures separated from one another and the source plate;

pillar structures vertically extending through the stack structure and contacting the discrete conductive structures of the source tier;

access line contact structures on the steps of the staircase structure and horizontally alternating with some of the pillar structures;

data lines overlying the stack structure;

an array of vertically extending strings of memory cells extending through the stack structure and electrically connected to the source plate and the data lines;

access lines electrically connected to the access line contact structures; and

a control device comprising CMOS circuitry vertically underlying the source tier and within horizontal boundaries of the array of vertically extending strings of memory cells, the control device electrically coupled to the source plate, the data lines, and the access lines.

21. The memory device of claim 20, wherein:

pillar structures have oblong horizontal cross-sectional shapes; and

horizontal centers of the pillar structures are offset from horizontal centers of the discrete

conductive structures in contact therewith.

22. The memory device of one of claims 20 and 21, wherein the dielectric-filled trenches are at least partially filled with aluminum oxide.

23. The memory device of one of claims 20 and 21, further comprising additional dielectric-filled trenches horizontally alternating with the dielectric-filled trenches and vertically extending completely through the stack structure, the additional dielectric-filled trenches dividing the stack structure into multiple blocks, and the dielectric-filled trenches dividing each of the blocks into multiple sub-blocks.

24. An electronic system, comprising:

an input device;

an output device;

a processor device operably coupled to the input device and the output device; and

a memory device operably coupled to the processor device and comprising a microelectronic device structure comprising:

a stack structure comprising tiers each comprising a conductive structure and a dielectric structure vertically neighboring the conductive structure;

trenches vertically extending completely through the stack structure and filled with dielectric material;

additional trenches horizontally alternating with the trenches and vertically extending partially through the stack structure, at least one of the additional trenches filled with additional dielectric material and comprising:

a lower portion; and

an upper portion having one or more greater horizontal widths than the lower portion;

a source tier vertically below the stack structure and comprising:

a source structure; and

discrete conductive structures electrically isolated from one another and the source structure; and

conductive pillars vertically extending through the stack structure to the discrete conductive structures of the source tier.

25. The electronic system of claim 24, wherein the memory device comprises a multi-deck 3D NAND Flash memory device.