## CLAIMS

What is claimed is:

1. An electronic interposer, comprising:

an upper section having between two and four upper section layers, wherein each upper section layer comprises an organic material, and at least one upper section conductive route comprising at least one upper section conductive trace and at least one upper section conductive via;

a lower section having between two and four lower section layers, wherein each lower section layer comprises an organic material, and at least one lower section conductive route comprising at least one lower section conductive trace and at least one lower section conductive via; and

a middle section between the upper section and the lower section, wherein the middle section comprises up to eight middle section layers, wherein each middle section layer comprises an organic material, and at least one middle section conductive route comprising at least one middle section conductive trace and at least one middle section conductive via, wherein a thickness of each middle section layer is less than a thickness of any the upper section layer and less than a thickness of any lower section layer, and wherein a thickness of the at least one middle section conductive trace is less than a thickness of the at least one upper section conductive trace and less than a thickness of the at least one lower section conductive trace.

2. The electronic interposer of claim 1, wherein the thickness of the upper section layers is between 13 and 40 microns, wherein the thickness of the lower section layers is between 13 and 40 microns, and wherein the thickness of the middle section layers is between 1.5 and 9 microns.

3. The electronic interposer of claim 1, wherein the at least one upper section conductive trace comprises a plurality of upper section conductive traces having a width of 8 microns or greater, a spacing of 8 microns or greater, and a thickness of between 8 and 15 microns; wherein the at least one lower section conductive trace comprises a plurality of lower section conductive traces having a width of 8 microns or greater, a spacing of 8 microns or greater, and a thickness of between 8 and 15 microns; and wherein the at least one middle section conductive trace comprises a plurality of middle section conductive traces having a width between 0.75 microns and 3 microns, a spacing between 0.75 microns and 3 microns, and a thickness of between 0.5 microns and 4 microns, and wherein the at least one middle section conductive via has a thickness of between 1 and 6 microns.

4. The electronic interposer of claim 1, further comprising at least one high-density device-to-device conductive route within the middle section.

5. The electronic interposer of claim 1, wherein the at least one middle section conductive trace has a thickness which allows general/coarse routing within the at least one middle section layer.

6. The electronic interposer of claim 1, further comprising at least one capacitor within at least one of the upper section and the lower section.

7. The electronic interposer of claim 1, wherein the upper section layers, the middle section layers, and the lower section layers have a coefficient of thermal expansion of between 9 and 25 ppm/° C. and an elastic moduli of between 1 and 20 GPa.

8. An integrated circuit package, comprising:

an electronic interposer, comprising:

an upper section having between two and four upper section layers, wherein each upper section layer comprises an organic material and at least one upper section conductive route comprising at least one upper section conductive trace and at least one upper section conductive via;

a lower section having between two and four lower section layers, wherein each lower section layer comprises an organic material and at least one lower section conductive route comprising at least one lower section conductive trace and at least one lower section conductive via; and

a middle section between the upper section and the lower section, wherein the middle section comprises up to eight middle section layers, wherein each middle section layer comprises an organic material and at least one middle section conductive route comprising at least one middle section conductive trace and at least one middle section conductive via, and wherein a thickness of each middle section layer is less than a thickness of any upper section layer and less than a thickness of any lower section layer, and wherein a

thickness of the at least one middle section conductive trace is less than a thickness of the at least one upper section conductive trace and less than a thickness of the at least one lower section conductive trace; and

a plurality of die side integrated circuit devices electrically attached to the upper section of the electronic interposer.

9. The integrated circuit package of claim 8, wherein the thickness of the upper section layers is between 13 and 40 microns, wherein the thickness of the lower section layers is between 13 and 40 microns, and wherein the thickness of the middle section layers is between 1.5 and 9 microns.

10. The integrated circuit package of claim 8, wherein the at least one upper section conductive trace comprises a plurality of conductive traces having a width of 8 microns or greater, a spacing of 8 microns or greater, and a thickness of between 8 and 15 microns; wherein the at least one lower section conductive trace comprises a plurality of conductive traces having a width of 8 microns or greater, a spacing of 8 microns or greater, and a thickness of between 8 and 15 microns; and wherein the at least one middle section conductive trace comprises a plurality of middle section conductive traces having a width between 0.75 microns and 3 microns, a spacing between 0.75 microns and 3 microns, and a thickness of between 0.5 microns and 4 microns, and wherein the at least one middle section conductive via has a thickness of between 1 and 6 microns.

11. The integrated circuit package of claim 8, further comprising at least one high-density device-to-device conductive route within the middle section which electrically interconnects one die side integrated circuit device of the plurality of die side integrated circuit devices with another die side integrated circuit device of the plurality of die side integrated circuit devices.

12. The integrated circuit package of claim 8, wherein the at least one middle section conductive trace thickness which allows general/coarse routing within the at least one middle section layer.

13. The integrated circuit package of claim 8, further comprising at least one land side integrated circuit device electrically attached to the lower section of the electronic interposer.

14. The integrated circuit package of claim 13, wherein the at least one land side integrated circuit device comprises a plurality of land side integrated circuit devices; and further comprising at least one high-density device-to-device conductive route within the middle section which electrically interconnects one land side integrated circuit device of the plurality of land side integrated circuit devices with another land side integrated circuit device of the plurality of land side integrated circuit devices.

15. The integrated circuit package of claim 13, wherein the at least one land side integrated circuit device is embedded in the lower section of the electronic interposer.

16. The integrated circuit package of claim 15, wherein the at least one land side integrated circuit device comprises a plurality of land side integrated circuit devices; and further comprising at least one high-density device-to-device conductive route within the middle section which electrically interconnects one land side integrated circuit device of the plurality of land side integrated circuit devices with another land side integrated circuit device of the plurality of land side integrated circuit devices.

17. An electronic system comprising:

a board; and

an integrated circuit package electrically attached to the board, wherein the integrated circuit package comprises:

an electronic interposer, comprising an upper section having between two and four upper section layers, wherein each upper section layer comprises an organic material and at least one upper section conductive route comprising at least one upper section conductive trace and at least one upper section conductive via; a lower section having between two and four lower section layers, wherein each lower section layer comprises an organic material and at least one lower section conductive route comprising at least one lower section conductive trace and at least one lower section conductive via; and a middle section between the upper section and the lower section, wherein the middle section comprises up to eight middle section layers, wherein each middle section layer comprises an organic material and at least one middle section conductive route comprising at least one middle section conductive trace and at least one middle section conductive via, wherein a thickness of each middle section layer is less than a thickness of any upper section layer and

less than a thickness of any lower section layer, and wherein a thickness of the at least one middle section conductive trace is less than a thickness of the at least one upper section conductive trace and less than a thickness of the at least one lower section conductive trace; and

a plurality of die side integrated circuit devices electrically attached to the upper section of the electronic interposer.

18. The electronic system of claim 17, wherein the thickness of the upper section layers is between 13 and 40 microns, wherein the thickness of the lower section layers is between 13 and 40 microns, and wherein the thickness of the middle section layers is between 1.5 and 9 microns.

19. The electronic system of claim 17, wherein the at least one upper section conductive trace comprises a plurality of upper section conductive traces having a width of 8 microns or greater, a spacing of 8 microns or greater, and a thickness of between 8 and 15 microns; wherein the at least one lower section conductive trace comprises a plurality of lower section conductive traces having a width of 8 microns or greater, a spacing of 8 microns or greater, and a thickness of between 8 and 15 microns; and wherein the at least one middle section conductive trace comprises a plurality of conductive traces having a width between 0.75 microns and 3 microns, a spacing between 0.75 microns and 3 microns, and a thickness of between 0.5 microns and 4 microns, and wherein the at least one middle section conductive via has a thickness of between 1 and 6 microns.

20. The electronic system of claim 17, further comprising at least one high-density device-to-device conductive route within the middle section which electrically interconnects one die side integrated circuit device of the plurality of die side integrated circuit devices with another die side integrated circuit device of the plurality of die side integrated circuit devices.

21. The electronic system of claim 17, wherein the at least one middle section conductive trace has thickness which allows general/coarse routing within the at least one middle section layer.

22. The electronic system of claim 17, further comprising at least one land side integrated circuit device electrically attached to the lower section of the electronic interposer.

23. The electronic system of claim 22, wherein the at least one land side integrated circuit device comprises a plurality of land side integrated circuit devices; and further comprising at least one high-density device-to-device conductive route within the middle section which electrically interconnects one land side integrated circuit device of the plurality of land side integrated circuit devices with another land side integrated circuit device of the plurality of land side integrated circuit devices.

24. The electronic system of claim 22, wherein the at least one land side integrated circuit device is embedded in the lower section of the electronic interposer.

25. The electronic system of claim 24, wherein the at least one land side integrated circuit device comprises a plurality of land side integrated circuit devices; and further comprising at least one high-density device-to-device conductive route within the middle section which electrically interconnects one land side integrated circuit device of the plurality of land side integrated circuit devices with another land side integrated circuit device of the plurality of land side integrated circuit devices.