CLAIMS

[Claim 1]

A semiconductor structure, comprising:

a carrier substrate, wherein the carrier substrate comprises a silicon substrate;

a trap-rich layer, disposed on the carrier substrate;

a dielectric layer, disposed on the trap-rich layer;

an interconnect structure, disposed on the dielectric layer;

a device structure layer, disposed on the interconnect structure and electrically connected to the interconnect structure; and

a circuit structure, disposed on the device structure layer and electrically connected to the device structure layer.

[Claim 2]

The semiconductor structure of claim 1, wherein the trap-rich layer comprises a polysilicon layer, an amorphous silicon layer, a silicon nitride layer, a silicon carbon nitride layer or a combination thereof.

[Claim 3]

The semiconductor structure of claim 1, wherein a thickness of the trap-rich layer is between 3000 Å and 20000 Å.

[Claim 4]

The semiconductor structure of claim 1, wherein the dielectric layer comprises an oxide silicon layer.

[Claim 5]

The semiconductor structure of claim 1, wherein a thickness of the dielectric layer is between 2000 Å and 8000 Å.

[Claim 6]

A manufacturing method of a semiconductor structure, comprising:

forming a trap-rich layer on a carrier substrate, wherein the carrier substrate comprises a silicon substrate;

forming a first dielectric layer on the trap-rich layer;

planarizing the first dielectric layer;

forming a device structure layer on an SOI substrate, wherein the SOI substrate comprises a silicon base and an insulating layer and a silicon layer sequentially stacked on the silicon base;

forming an interconnect structure on the device structure layer, wherein the interconnect structure is electrically connected to the device structure layer;

forming a second dielectric layer on the interconnect structure;

bonding the carrier substrate and the SOI substrate in a manner that the first dielectric layer faces the second dielectric layer;

removing the silicon base of the SOI substrate; and

forming a circuit structure on the insulating layer, wherein the circuit structure is electrically connected to the device structure layer.

[Claim 7]

The manufacturing method of a semiconductor structure of claim 6, wherein the trap-rich layer comprises a polysilicon layer, an amorphous silicon layer, a silicon nitride layer, a silicon carbon nitride layer or a combination thereof.

[Claim 8]

The manufacturing method of a semiconductor structure of claim 6, wherein a thickness of the trap-rich layer is between 3000 Å and 20000 Å.

[Claim 9]

The manufacturing method of a semiconductor structure of claim 6, wherein a thickness of the planarized first dielectric layer is between 500 Å and 5000 Å.

[Claim 10]

The manufacturing method of a semiconductor structure of claim 6, wherein the first dielectric layer comprises a silicon oxide layer.

[Claim 11]

The manufacturing method of a semiconductor structure of claim 6, wherein the second dielectric layer comprises a silicon oxide layer.

[Claim 12]

The manufacturing method of a semiconductor structure of claim 6, wherein the method for planarizing the first dielectric layer comprises performing a chemical mechanical polishing process.

[Claim 13]

The manufacturing method of a semiconductor structure of claim 6, wherein the method for removing the silicon base of the SOI substrate comprises:

thinning the silicon base; and

perform an etching process on the thinned silicon base.