WHAT IS CLAIMED IS:

1. A method of operating a memory system, the memory system including a non-volatile memory, the method comprising:

measuring, using processing circuitry, an erase program interval (EPI) of a memory group, the EPI being a time period from an erase time point to a program time point of the memory group, the memory group included in the non-volatile memory;

determining, using the processing circuitry, a plurality of program modes based on a number of data bits stored in each memory cell of the memory group;

selecting, using the processing circuitry, a program mode for the memory group from the plurality of program modes, based on the measured EPI of the memory group; and

performing, using the processing circuitry, a program operation on the memory group corresponding to the selected program mode, the performing the program operation on the memory group including adjusting at least one voltage level of the program operation based on the selected program mode.

2. The method of claim 1, wherein

the plurality of program modes comprise at least one of a quadruple-level cell (QLC) mode, a triple level cell (TLC) mode, a multi-level cell (MLC) mode, and a single level cell (SLC) mode, or combinations thereof.

3. The method of claim 1 or claim 2, wherein

the memory group comprises at least one of a memory block, a memory stack, and a sub-memory block, or combinations thereof.

4. The method of claims 1 or claim 2, wherein

the memory group includes a memory block; and

the selecting the program mode comprises,

selecting the program mode for the memory block as a first program mode in which N-bit data is written to each memory cell, in response to the measured EPI being equal to, or shorter than, a reference time, and

selecting the program mode for the memory block as a second program

mode in which M-bit data is written to each memory cell, in response to the measured EPI exceeding the reference time,

wherein N and M are positive integers, and M is less than N.

5. The method of claim 1, wherein

the non-volatile memory comprises a plurality of memory blocks, each memory block of the plurality of memory blocks comprising a plurality of memory stacks stacked on a substrate in a perpendicular direction to a substrate of the non-volatile memory;

the memory group includes a memory stack;

the measuring of the EPI of the memory group comprises,

measuring a first EPI of a first memory stack of the memory group, and

measuring a second EPI of a second memory stack of the memory group, the second memory stack located on the first memory stack in a perpendicular direction to the first memory stack; and

the selecting of the program mode comprises,

selecting a program mode for the first memory stack as at least one of quadruple level cell (QLC) mode, a triple level cell (TLC) mode, a multi-level cell (MLC) mode, and a single level cell (SLC) mode, based on the first EPI.

6. The method of claim 5, wherein the selecting of the program mode further comprises:

selecting a program mode for the second memory stack as at least one of the QLC mode, the TLC mode, the MLC mode, and the SLC mode, based on the second EPI, in response to the first EPI exceeding a reference time during a program operation performed on the first memory stack.

7. The method of claim 1, wherein

the non-volatile memory comprises a plurality of memory blocks, each of the memory blocks of the plurality of memory blocks including a plurality of sub-memory blocks that are independently erasable;

the measuring of the EPI of the memory group comprises,

measuring a first EPI of a first sub-memory block, and

measuring a second EPI of a second sub-memory block located adjacent to the first sub-memory block; and

the selecting the program mode comprises,

selecting a program mode for the first sub-memory block as at least one of a quadruple level cell (QLC) mode, a triple level cell (TLC) mode, a multi-level cell (MLC) mode, and a single level cell (SLC) mode, based on the first EPI.

8. The method of claim 7, wherein the selecting the program mode further comprises:

selecting a program mode for the second sub-memory block as at least one of the QLC mode, the TLC mode, the MLC mode, and the SLC mode, based on the second EPI, in response to the first EPI exceeding a reference time during a program operation performed on the first sub-memory block.

9. The method of any one of claims 1 to 8, wherein

the non-volatile memory comprises a meta region configured to store an EPI table in which EPI information indicating the measured EPI corresponding to each memory group is stored; and

the measuring of the EPI of the memory group comprises measuring the EPI corresponding to the memory group based on the EPI table stored in the meta region.

10. The method of any one of claims 1 to 9, further comprising:

selecting, using the processing circuitry, a program mode for the memory group, the selecting the program mode for the memory group including selecting a default program mode after occurrence of a sudden power-off (SPO) event, the default program mode being a multi-level cell (MLC) mode or a single level cell (SLC) mode.

11. The method of any one of claims 1 to 10, wherein the measuring of the EPI of the memory group comprises at least one of:

measuring the EPI of the memory group during a user data program operation in response to a write request received from a host;

measuring the EPI of the memory group during a meta data program operation;

measuring the EPI of the memory group during a garbage collection operation; or

combinations thereof.

12. The method of any one of claims 1 to 11, further comprising:

selecting a program mode corresponding to a memory block of the memory group, based on a program mode table in response to a read request for the memory group, the program mode table including a program mode corresponding to each memory group; and

adjusting a read condition for the memory group based on the selected program mode for the memory block of the memory group, the adjusting the read condition including adjusting at least one voltage level associated with the read condition based on the selected program mode of the memory block.

13. A method of operating a memory system, the memory system including a non-volatile memory, the method comprising:

measuring, using processing circuitry, an erase program interval (EPI) of a memory block of the non-volatile memory in response to a write request received from a host, the EPI being a time period from an erase time point to a program time point of the memory block; and

performing, using the processing circuitry, a program operation on the memory block in at least one program mode based on a duration of the EPI, the at least one program mode including a first program mode and a second program mode, the first program mode including writing N-bit data to each memory cell of the memory block, and the second program mode including writing M-bit data to each memory cell of the memory block, the performing the program operation on the memory block including adjusting at least one voltage level of the program operation based on the first program mode or the second program mode,

wherein N and M are positive integers, and M is less than N.

14. The method of claim 13, wherein

the at least one program mode further includes a third program mode; and

the performing the program operation on the memory block further includes: performing, using the processing circuitry, the program operation on the memory block in

the third program mode in response to the EPI exceeding a first reference time and a second reference time, the third program mode including writing L-bit data to each memory cell of the memory block, the second reference time being longer than the first reference time,

wherein L is a positive integer less than M.

15. The method of claim 14, wherein

the at least one program mode further includes a fourth program mode; and

the performing the program operation on the memory block further includes: performing, using the processing circuitry, the program operation on the memory block in the fourth program mode in response to the EPI exceeding a third reference time, the third reference time being longer than the second reference time, the fourth program mode including writing K-bit data to each memory cell of the memory block, wherein K is a positive integer less than L.

16. The method of any one of claims 13 to 15, wherein

the measuring of the EPI of the memory block comprises reading the EPI of the memory block from an EPI table stored in a meta region of the non-volatile memory.

17. The method of any one of claims 13 to 16, further comprising:

selecting, using the processing circuitry, a program mode corresponding to the memory block based on a program mode table in response to a read request for the memory block, the program mode table including a program mode corresponding to each memory block; and

adjusting, using the processing circuitry, a read condition for the memory block based on the selected program mode of the memory block, the adjusting the read condition including adjusting at least one voltage level associated with the read condition based on the selected program mode of the memory block.

18. A memory system comprising:

a non-volatile memory comprising a plurality of memory groups; and

a memory controller configured to,

measure an erase program interval (EPI) of a first memory group from

among the plurality of memory groups, the EPI being a time period from an erase time point to a program time point of the memory group,

determine a plurality of program modes based on a number of data bits stored in each memory cell of the memory group,

select a program mode for the first memory group from the plurality of program modes based on the measured EPI, and

control a program operation on the first memory group based on the selected program mode of the first memory group, the controlling the program operation including adjusting at least one voltage level associated with the program operation based on the selected program mode.

19. The memory system of claim 18, wherein

the plurality of program modes comprise at least one of a quadruple level cell (QLC) mode, a triple level cell (TLC) mode, a multi-level cell (MLC) mode, and a single level cell (SLC) mode.

20. The memory system of claim 18 or claim 19, wherein

the memory group comprises a memory block, a memory stack, a sub-memory block, or combinations thereof.