WHAT IS CLAIMED IS:

1. A nonvolatile memory device comprising:

a memory cell array disposed on a substrate, wherein the memory cell array comprises a plurality of memory blocks;

a row decoder connected to the memory cell array through word lines; and

a page buffer connected to the memory cell array through bit lines,

wherein each of the memory blocks comprises a pillar including a first portion disposed on the substrate and a second portion stacked on the first portion,

wherein a width of the first portion increases as a distance from the substrate increases, and first conductive materials and first insulating layers surround the first portion and are stacked in turn on the substrate,

wherein a width of the second portion increases as a distance from the substrate increases, and second conductive materials and second insulating layers surround the second portion and are stacked in turn on the substrate,

wherein a first boundary is located between the first portion and the second portion,

wherein the first conductive materials form first memory cells together with the first portion and the second conductive materials form second memory cells together with the second portion, and

wherein, when performing program operations based on consecutive addresses in a selected memory block of the memory blocks, the row decoder and the page buffer are configured to complete a second program operation of an adjacent memory cell adjacent to the first boundary after sequentially completing first program operations of non-adjacent memory cells not adjacent to the first boundary from among the first and second memory cells.

2. The nonvolatile memory device of claim 1, wherein the adjacent memory cell includes a memory cell closest to the first boundary from among the first memory cells.

3. The nonvolatile memory device of claim 1 or claim 2, wherein the first program operations include third program operations of first non-adjacent memory cells belonging to the first portion from among the non-adjacent memory cells and fourth program operations of second non-adjacent memory cells belonging to the second portion from among the non-adjacent memory cells,

wherein the second program operation includes a 1-step program operation and a 2-step program operation, and

wherein the row decoder and the page buffer are further configured to:

complete one of the third program operations and the fourth program operations;

perform the 1-step program operation;

complete the other of the third program operations and the fourth program operations; and

then perform the 2-step program operation.

4. The nonvolatile memory device of any one of claims 1 to 3, wherein the adjacent memory cell includes a memory cell closest to the first boundary from among the second memory cells.

5. The nonvolatile memory device of claim 1, wherein the adjacent memory cell includes a memory cell closest to the first boundary from among the first memory cells and a memory cell closest to the first boundary from among the second memory cells.

6. The nonvolatile memory device of claim 5, wherein the first program operations include third program operations of first non-adjacent memory cells belonging to the first portion from among the non-adjacent memory cells and fourth program operations of second non-adjacent memory cells belonging to the second portion from among the non-adjacent memory cells,

wherein the second program operation includes a fifth program operation of a first adjacent memory cell and a sixth program operation of a second adjacent memory cell,

wherein each of the fifth program operation and the sixth program operation includes a 1-step program operation and a 2-step program operation, and

wherein the row decoder and the page buffer are further configured to:

complete one of the third program operations and the fourth program operations;

perform the 1-step program operation of each of the fifth and sixth program operations;

complete the others of the third program operations and the fourth program operations; and

then perform the 2-step program operation of each of the fifth and sixth program operations.

7. The nonvolatile memory device of claim 1, wherein the pillar further comprises a third portion stacked on the second portion,

wherein a width of the third portion increases as a distance from the substrate increases, and third conductive materials and third insulating layers surround the third portion and are stacked in turn on the substrate,

wherein a second boundary is located between the second portion and the third

portion, and

wherein the third conductive materials form third memory cells together with the third portion.

8. The nonvolatile memory device of claim 7, wherein the row decoder and the page buffer are further configured to:

complete programming of the third memory cells;

then complete programming of fifth memory cells being remaining memory cells of the second memory cells other than a fourth memory cell closest to the second boundary, and seventh memory cells being remaining memory cells of the first memory cells other than a sixth memory cell closest to the first boundary, through the first program operations;

then complete programming of the fourth memory cell; and

then complete programming of the sixth memory cell through the second program operation.

9. The nonvolatile memory device of claim 8, wherein the second program operation includes a 1-step program operation and a 2-step program operation, and

wherein the row decoder and the page buffer are further configured to:

perform the 1-step program operation of the sixth memory cell after completing programming of the fifth memory cells;

then complete programming of the seventh memory cells; and

then perform the 2-step program operation on the sixth memory cell.

10. The nonvolatile memory device of claim 7, wherein the row decoder and the page buffer are further configured to:

complete programming of the third memory cells;

then complete programming of fifth memory cells being remaining memory cells of the second memory cells other than a fourth memory cell closest to the second boundary, through a part of the first program operations;

then complete programming of the fourth memory cell;

then complete programming of seventh memory cells being remaining memory cells of the first memory cells other than a sixth memory cell closest to the first boundary, through the others of the first program operations; and

then complete programming of the sixth memory cells through the second program operation.

11. The nonvolatile memory device of claim 10, wherein the second program operation includes a 1-step program operation and a 2-step program operation, and

wherein the row decoder and the page buffer are further configured to:

perform the 1-step program operation on the sixth memory cell after completing programming of the fifth memory cells;

then complete programming of the seventh memory cells; and

then perform the 2-step program operation on the sixth memory cell.

12. The nonvolatile memory device of claim 7, wherein the row decoder and the page buffer are further configured to:

complete programming of fifth memory cells being remaining memory cells of the third memory cells other than a fourth memory cell closest to the second boundary;

then complete programming of eighth memory cells being remaining memory cells of the second memory cells other than a sixth memory cell closest to the second boundary

and a seventh memory cell closest to the first boundary, through a part of the first program operations;

then complete programming of tenth memory cells being remaining memory cells of the first memory cells other than a ninth memory cell closest to the first boundary, through the others of the first program operations;

then complete programming of the fourth memory cell and the sixth memory cell; and

then complete programming of the seventh memory cell and the ninth memory cell through third program operations including the second program operation.

13. The nonvolatile memory device of claim 12, wherein the third program operations include 1-step program operations and 2-step program operations, and

wherein the row decoder and the page buffer are further configured to:

perform the 1-step program operations on the seventh memory cell and the ninth memory cell after completing programming of the eighth memory cells;

then complete programming of the tenth memory cells; and

then perform the 2-step program operations on the seventh memory cell and the ninth memory cell.

14. The nonvolatile memory device of claim 7, wherein the row decoder and the page buffer are further configured to:

complete programming of fifth memory cells being remaining memory cells of the third memory cells other than a fourth memory cell closest to the second boundary;

then complete programming of eighth memory cells being remaining memory cells of the second memory cells other than a sixth memory cell closest to the second boundary

and a seventh memory cell closest to the first boundary, through a part of the first program operations;

then complete programming of the fourth memory cell and the sixth memory cell;

then complete programming of tenth memory cells being remaining memory cells of the first memory cells other than a ninth memory cell closest to the first boundary, through the others of the first program operations; and

then complete programming of the seventh memory cell and the ninth memory cell through third program operations including the second program operation.

15. The nonvolatile memory device of claim 7, wherein the row decoder and the page buffer are further configured to:

complete programming of fifth memory cells being remaining memory cells of the third memory cells other than a fourth memory cell closest to the second boundary;

then complete programming of seventh memory cells being remaining memory cells of the second memory cells other than a sixth memory cell closest to the first boundary, through a part of the first program operations;

then complete programming of the first memory cells through the others of the first program operations;

then complete programming of the fourth memory cell; and

then complete programming of the sixth memory cell through the second program operation.

16. The nonvolatile memory device of claim 7, wherein the row decoder and the page buffer are further configured to:

complete programming of fifth memory cells being remaining memory cells of the

third memory cells other than a fourth memory cell closest to the second boundary;

then complete programming of seventh memory cells being remaining memory cells of the second memory cells other than a sixth memory cell closest to the first boundary, through a part of the first program operations;

then complete programming of the fourth memory cell;

then complete programming of the first memory cells through the others of the first program operations; and

then complete programming of the sixth memory cell through the second program operation.

17. A storage device comprising:

a nonvolatile memory device including a plurality of memory blocks; and

a controller configured to control a write operation for a selected memory block of the memory blocks of the nonvolatile memory device,

wherein each of the memory blocks comprises:

first memory cells corresponding to a first portion of a pillar extending in a direction perpendicular to a substrate; and

second memory cells corresponding to a second portion of the pillar extending in the direction perpendicular to the substrate and disposed on the first portion,

wherein the first memory cells and the second memory cells are classified into at least one first adjacent memory cell adjacent to a first boundary between the first portion and the second portion and first non-adjacent memory cells being remaining memory cells other than the at least one first adjacent memory cell,

wherein, in the write operation of the selected memory block, the controller controls the nonvolatile memory device such that a program operation of the at least one

first adjacent memory cell is completed after a program operation of the first non-adjacent memory cells is completed, and the number of bits to be written in the at least one first adjacent memory cell is smaller than the number of bits to be written in each of the first non-adjacent memory cells when program operations of the first memory cells and the second memory cells are completed.

18. The storage device of claim 17, wherein, as a use cycle of the selected memory block increases, the controller decreases the number of the bits to be written in the first adjacent memory cell.

19. The storage device of claim 17 or claim 18, wherein each of the memory blocks further comprises third memory cells corresponding to a third portion of the pillar extending in the direction perpendicular to the substrate and disposed on the second portion,

wherein the second memory cells and the third memory cells are classified into at least one second adjacent memory cell adjacent to a second boundary between the second portion and the third portion and second non-adjacent memory cells being remaining memory cells other than the at least one second adjacent memory cell, and

wherein the controller differently controls the number of bits to be written in the first non-adjacent memory cell and the number of bits to be written in the second non-adjacent memory cell.

20. An operating method of a nonvolatile memory device including memory cells connected in series between a string selection transistor and a ground selection transistor, the method comprising:

completing first program operations of first memory cells of the memory cells; and

completing a second program operation of at least one second memory cell located between the first memory cells, after completing the first program operations of the first memory cells,

wherein the memory cells are stacked in a direction perpendicular to a substrate, based on a first portion of a pillar extending in the direction perpendicular to the substrate and a second portion of the pillar extending in the direction perpendicular to the substrate and disposed on the first portion, and

wherein the at least one second memory cell is adjacent to a boundary between the first portion and the second portion.