WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array including a plurality of memory cells;

a peripheral circuit configured to perform a program operation on selected memory cells among the plurality of memory cells;

control logic configured to control an operation of the peripheral circuit,

wherein the control logic controls the peripheral circuit to perform a pre-program operation on first memory cells to be programmed to an upper programmed state among the selected memory cells and perform a normal program operation on the selected memory cells after the pre-program operation.

2. The semiconductor memory device according to claim 1, wherein, during the pre-program operation, the control logic controls the peripheral circuit to apply a program enable voltage to each of bit lines coupled with the first memory cells, apply a program inhibit voltage to each of bit lines coupled with second memory cells other than the first memory cells among the selected memory cells, and apply a pre-program pulse to a selected word line coupled with the selected memory cells.

3. The semiconductor memory device according to claim 2, wherein the program enable voltage is a voltage lower than the program inhibit

voltage.

4. The semiconductor memory device according to claim 2, wherein the control logic controls the peripheral circuit such that a program pass voltage is applied to an unselected word line while the pre-program pulse is applied to the selected word line.

5. The semiconductor memory device according to claim 2, wherein the control logic controls the peripheral circuit such that, while the pre-program pulse is applied to the selected word line, a first program pass voltage is applied to a first unselected word line disposed adjacent to the selected word line, and a second program pass voltage is applied to a second unselected word line other than the first unselected word line.

6. The semiconductor memory device according to claim 5, wherein a voltage level of the first program pass voltage is greater than a voltage level of the second program pass voltage.

7. The semiconductor memory device according to claim 1,

wherein each of the plurality of memory cells comprises a multi-level cell configured to store 2-bit data, and each of the selected memory cells is programmed to have a threshold voltage corresponding to any one of an erased state and first to third programmed states, and

wherein the upper programmed state includes the third

programmed state.

8. The semiconductor memory device according to claim 1,

wherein each of the plurality of memory cells comprises a multi-level cell configured to store 2-bit data, and each of the selected memory cells is programmed to have a threshold voltage corresponding to any one of an erased state, a first programmed state, a second programmed state, and a third programmed state, and

wherein the upper programmed state includes the second and the third programmed states.

9. The semiconductor memory device according to claim 1,

wherein each of the plurality of memory cells comprises a triple-level cell configured to store 3-bit data, and each of the selected memory cells is programmed to have a threshold voltage corresponding to any one of an erased state and first to seventh programmed states, and

wherein the upper programmed state includes the seventh programmed state.

10. The semiconductor memory device according to claim 1,

wherein each of the plurality of memory cells comprises a triple-level cell configured to store 3-bit data, and each of the selected memory cells is programmed to have a threshold voltage corresponding to any one of an erased state and first to seventh programmed states, and

wherein the upper programmed state includes the sixth and the seventh programmed states.

11. A method of operating a semiconductor memory device including a plurality of memory cells, the method comprising:

performing a pre-program operation on at least some memory cells included in a selected physical page among the plurality of memory cells; and

performing a normal program operation on the memory cells included in the selected physical page,

wherein performing the pre-program operation comprises pre-programming memory cells to be programmed to an upper programmed state among the memory cells included in the selected physical page.

12. The method according to claim 11, wherein performing the pre-program operation comprises:

setting respective bit line voltages to be applied to bit lines coupled with the memory cells included in the selected physical page;

setting program pass voltages to be applied to unselected word lines that are not coupled with the selected physical page; and

applying a pre-program pulse to a selected word line coupled with the selected physical page.

13. The method according to claim 12, wherein setting the respective bit line voltages comprises:

applying a program enable voltage to each of bit lines coupled with first memory cells to be programmed to the upper programmed state among the memory cells included in the selected physical page; and

applying a program inhibit voltage to each of bit lines coupled with second memory cells other than the first memory cells among the memory cells included in the selected physical page.

14. The method according to claim 12, wherein setting the program pass voltages comprises:

applying a first program pass voltage to each of first unselected word lines disposed adjacent to the selected word line among the unselected word lines; and

applying a second program pass voltage to each of second unselected word lines other than the first unselected word lines among the unselected word lines.

15. The method according to claim 14, wherein a voltage level of the first program pass voltage is greater than a voltage level of the second program pass voltage.

16. The method according to claim 11,

wherein each of the plurality of memory cells comprises a multi-

level cell configured to store 2-bit data, and each of the selected memory cells is programmed to have a threshold voltage corresponding to any one of an erased state and first to third programmed states, and

wherein the upper programmed state includes the third programmed state.

17. The method according to claim 11,

wherein each of the plurality of memory cells comprises a multi-level cell configured to store 2-bit data, and each of the selected memory cells is programmed to have a threshold voltage corresponding to any one of an erased state, a first programmed state, a second programmed state, and a third programmed state, and

wherein the upper programmed state includes the second and the third programmed states.

18. The method according to claim 11,

wherein each of the plurality of memory cells comprises a triple-level cell configured to store 3-bit data, and each of the selected memory cells is programmed to have a threshold voltage corresponding to any one of an erased state and first to seventh programmed states, and

wherein the upper programmed state includes the seventh programmed state.

19. The method according to claim 11,

wherein each of the plurality of memory cells comprises a triple-level cell configured to store 3-bit data, and each of the selected memory cells is programmed to have a threshold voltage corresponding to any one of an erased state and first to seventh programmed states, and

wherein the upper programmed state includes the sixth and the seventh programmed states.