9. The interface circuit of claim 1, further comprising M output buffer circuits in one-to-one correspondence with the data pads, each of the output buffer circuits being driven by the clock signal to transmit the data signals to the corresponding data pads.

10. The interface circuit of claim 9, wherein lengths of output data paths from each of the output buffer circuits to a data pad corresponding to each of the output buffer circuits are the same.

11. The interface circuit of claim 1, wherein each input buffer circuit comprises a multiplexer and a latch, the multiplexer receives the data signals, processes the data signals and outputs the processed data signals to the latch, and an output of the latch serves as an output of each input buffer circuit.

12. A data transmission circuit, comprising the interface circuit of any of claims 1-11, and further comprising:

M sequential-to-parallel conversion circuits, wherein the M sequential-to-parallel conversion circuits are in one-to-one correspondence with the M input buffer circuits, and an output of each of the input buffer circuits serves as an input of a corresponding sequential-to-parallel conversion circuit.

13. The data transmission circuit of claim 12, wherein the M sequential-to-parallel conversion circuits are arranged in a third row, and lengths of transmission paths between each of the input buffer circuits on the same side of the axis and a sequential-to-parallel conversion circuit corresponding to each of the input buffer circuits are different.

14. The data transmission circuit of claim 12, wherein the M sequential-to-parallel conversion

circuits are in one-to-one correspondence with the M data pads, and distances between each of the sequential-to-parallel conversion circuits and a data pad corresponding to each of the sequential-to-parallel conversion circuits are the same.

15. The data transmission circuit of claim 12, further comprising:

M First Input First Output (FIFO) circuits in one-to-one correspondence with the M sequential-to-parallel conversion circuits;

M parallel-to-sequential conversion circuits in one-to-one correspondence with the M FIFO circuits, wherein an output of each FIFO circuit serves as an input of the corresponding parallel-to-sequential conversion circuit; and

M driving circuits in one-to-one correspondence with the M parallel-to-sequential conversion circuits, wherein an output of each parallel-to-sequential conversion circuit serves as an input of a driving circuit corresponding to the parallel-to-sequential conversion circuit, and the M driving circuits are in one-to-one correspondence with the M data pads.

16. The data transmission circuit of claim 15, further comprising M optional input buffer circuits, wherein the M optional input buffer circuits have the same number as the input buffer circuits and are arranged side by side with the input buffer circuits.

17. The data transmission circuit of claim 16, wherein two of the M input buffer circuits and/or the M optional input buffer circuits, one of the M sequential-to-parallel conversion circuits, one of the M FIFO circuits, one of the M parallel-to-sequential conversion circuits and one of the M driving circuits jointly form a data transmission unit, and operating environments of each of the data transmission units are matched.

18. The data transmission circuit of claim 17, wherein the sequential-to-parallel conversion

circuits and the FIFO circuits in the same data transmission unit are arranged in side by side or in parallel.

19. The data transmission circuit of claim 17, wherein the FIFO circuits located in different data transmission units are arranged side by side.

20. A memory, comprising the data transmission circuit of any of claims 12-19.