WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

an element isolation structure having a first sidewall and a second sidewall extending in a first direction, the first sidewall being opposite to the second sidewall in a second direction;

a first fin-shaped pattern in contact with the first sidewall of the element isolation structure, the first fin-shaped pattern extending in the second direction;

a second fin-shaped pattern in contact with the first sidewall of the element isolation structure, the second fin-shaped pattern extending in the second direction and being spaced apart from the first fin-shaped pattern in the first direction;

a first gate electrode extending in the first direction and disposed on the first fin-shaped pattern;

a first source/drain contact disposed on the first fin-shaped pattern and the second fin-shaped pattern, the first source/drain contact extending in the first direction and disposed between the first gate electrode and the element isolation structure; and

a wiring structure connected to the first source/drain contact and disposed on the first source/drain contact,

wherein the first source/drain contact includes a first lower contact region that is disposed on the first fin-shaped pattern and the second fin-shaped pattern, a first upper contact region that is disposed on the first lower contact region, and a first dummy contact region, and

the wiring structure contacts an upper surface of the first upper contact region and is spaced apart from an upper surface of the first dummy contact region.

2. The semiconductor device as claimed in claim 1, wherein no gate electrode is disposed between the first source/drain contact and the element isolation structure.

3. The semiconductor device as claimed in claim 1 or claim 2, further comprising a first gate contact connected to the first gate electrode and disposed on the first gate electrode, the first gate contact not overlapping the first upper contact region and the first dummy contact region in the second direction.

4. The semiconductor device as claimed in any one of claims 1 to 3, wherein the first gate electrode is disposed on the second fin-shaped pattern.

5. The semiconductor device as claimed in any one of claims 1 to 4, further comprising:

a second gate electrode disposed on the second fin-shaped pattern and spaced apart from the first gate electrode in the first direction, the first source/drain contact being between the second gate electrode and the element isolation structure; and

a second gate contact connected to the second gate electrode and disposed on the second gate electrode, the second gate contact not overlapping the first upper contact region and the first dummy contact region in the second direction.

6. The semiconductor device as claimed in claim 5, further comprising a gate isolation structure disposed between the first gate electrode and the second gate electrode, the gate isolation structure not overlapping the first upper contact region and the first dummy contact region in the second direction.

7. The semiconductor device as claimed in any one of claims 1 to 6, further comprising:

a third fin-shaped pattern in contact with the second sidewall of the element isolation structure, the third fin-shaped pattern extending in the second direction;

a fourth fin-shaped pattern in contact with the second sidewall of the element isolation structure, the fourth fin-shaped pattern extending in the second direction and being spaced apart from the third fin-shaped pattern in the first direction; and

a second source/drain contact disposed on the third fin-shaped pattern and the fourth fin-shaped pattern,

wherein the second source/drain contact includes a second lower contact region that is disposed on the third fin-shaped pattern and the fourth fin-shaped pattern, and a second upper contact region that is disposed on the second lower contact region, an upper surface of the second upper contact region being in contact with the wiring structure.

8. The semiconductor device as claimed in claim 7, wherein the second source/drain contact further includes a second dummy contact region disposed on the second lower contact region, an upper surface of the second dummy contact region not being in contact with the wiring structure.

9. The semiconductor device as claimed in claim 7 or claim 8, wherein the second source/drain contact further includes a third upper contact region disposed on the second lower contact region, an upper surface of the third upper contact region being in contact with the wiring structure.

10. The semiconductor device as claimed in any one of claims 1 to 6, further comprising:

a third fin-shaped pattern in contact with the second sidewall of the element isolation structure, the third fin-shaped pattern extending in the second direction;

a fourth fin-shaped pattern in contact with the second sidewall of the element isolation structure, the fourth fin-shaped pattern extending in the second direction and being spaced apart from the third fin-shaped pattern in the first direction;

a second source/drain contact disposed on the third fin-shaped pattern; and

a third source/drain contact disposed on the fourth fin-shaped pattern, the second source/drain contact being spaced apart from the third source/drain contact in the first direction.

11. The semiconductor device as claimed in any one of claims 1 to 10, wherein:

the first lower contact region includes a connecting portion between the first upper contact region and the first dummy contact region, a first protruding portion, and a second protruding portion, and

the first upper contact region is disposed between the connecting portion and the first protruding portion, and the first dummy contact region is disposed between the connecting portion and the second protruding portion.

12. The semiconductor device as claimed in any one of claims 1 to 11, further comprising a sheet pattern spaced apart from the first fin-shaped pattern and disposed on the first fin-shaped pattern, the first gate electrode wrapping the sheet pattern.

13. A semiconductor device, comprising:

a first fin-shaped pattern extending in a first direction;

a second fin-shaped pattern extending in the first direction and spaced apart from the first fin-shaped pattern in a second direction;

a third fin-shaped pattern extending in the first direction;

a fourth fin-shaped pattern extending in the first direction and spaced apart from the third fin-shaped pattern in the second direction;

an element isolation structure extending in the second direction and in contact with the first fin-shaped pattern and the second fin-shaped pattern;

a first gate electrode extending in the second direction and disposed on the first fin-shaped pattern;

a second gate electrode extending in the second direction and disposed on the third fin-shaped pattern;

a third gate electrode extending in the second direction and disposed on the fourth fin-shaped pattern;

a first source/drain contact disposed on the first fin-shaped pattern and the second fin-shaped pattern and disposed between the first gate electrode and the element isolation structure, the first source/drain contact extending in the second direction;

a second source/drain contact disposed on the third fin-shaped pattern and fourth fin-shaped pattern, disposed between the second gate electrode and the element isolation structure, and disposed between the third gate electrode and the element isolation structure, the second source/drain contact extending in the second direction; and

a wiring structure disposed on the first source/drain contact and the second source/drain contact, the wiring structure being connected to the first source/drain contact and the second source/drain contact,

wherein:

the first source/drain contact includes a first lower contact region disposed on the first fin-shaped pattern and the second fin-shaped pattern, and a first upper contact region disposed on the first lower contact region,

the second source/drain contact includes a second lower contact region disposed on the third fin-shaped pattern and the fourth fin-shaped pattern, and a second upper contact region disposed on the second lower contact region,

the wiring structure includes a via plug in contact with the first upper contact region and the second upper contact region,

a bottom surface of the via plug has a first width,

a width of an upper surface of the first upper contact region is greater than or equal to 1.5 times the first width, and

a width of an upper surface of the second upper contact region is smaller than or equal to 1.2 times the first width.

14. The semiconductor device as claimed in claim 13, wherein the first source/drain contact includes a first dummy contact region disposed on the first lower contact region.

15. A semiconductor device, comprising:

a first fin-shaped pattern extending in a first direction;

a second fin-shaped pattern spaced apart from the first fin-shaped pattern in a second direction and extending in the first direction;

a third fin-shaped pattern spaced apart from the first fin-shaped pattern in the first direction and extending in the first direction;

a fourth fin-shaped pattern spaced apart from the second fin-shaped pattern in the first direction and extending in the first direction;

a first source/drain contact on the first fin-shaped pattern and the second fin-shaped pattern and extending in the second direction;

a second source/drain contact on the third fin-shaped pattern and the fourth fin-shaped pattern and extending in the second direction;

an element isolation structure disposed between the first fin-shaped pattern and the third fin-shaped pattern and disposed between the second fin-shaped pattern and the fourth fin-shaped pattern; and

a wiring structure disposed on the first source/drain contact and the second source/drain contact, and connected to the first source/drain contact and the second source/drain contact,

wherein:

the first source/drain contact includes a first lower contact region disposed on the first fin-shaped pattern and the second fin-shaped pattern, a first upper contact region disposed on the first lower contact region, and a first dummy contact region,

the second source/drain contact includes a second lower contact region disposed on the third fin-shaped pattern and the fourth fin-shaped pattern, and a second upper contact region disposed on the second lower contact region, and

the wiring structure is in contact with an upper surface of the first upper contact region and an upper surface of the second upper contact region, and is not in contact with an upper surface of the first dummy contact region.

16. The semiconductor device as claimed in claim 15, wherein the second source/drain contact further includes a second dummy contact region disposed on the second lower contact region, an upper surface of the second dummy contact region not being in contact with the wiring structure.

17. The semiconductor device as claimed in claim 15 or claim 16, further comprising: a first gate electrode disposed on the first fin-shaped pattern; and
a first gate contact disposed on the first gate electrode.

18. The semiconductor device as claimed in claim 17, further comprising:
a second gate electrode disposed on the third fin-shaped pattern;
a third gate electrode disposed on the fourth fin-shaped pattern; and
a gate isolation structure disposed between the second gate electrode and the third gate electrode.

19. The semiconductor device as claimed in claim 15, further comprising:
a first source/drain disposed on the first fin-shaped pattern; and
a second source/drain disposed on the second fin-shaped pattern,
wherein the first source/drain contact is disposed on the first source/drain and the second source/drain, and
a bottom surface of the first source/drain is disposed higher than a bottom surface of the element isolation structure.

20. The semiconductor device as claimed in claim 19, wherein the first lower contact region includes a first portion disposed on the first source/drain, a second portion disposed on the second source/drain and a third portion disposed between the first portion and the second portion, and
a bottom surface of the third portion is disposed lower than a bottom surface of the first portion and lower than a bottom surface of the second portion.