**[0054]** These and other features of the disclosed embodiments will be described in detail below with reference to the associated drawings.

## BRIEF DESCRIPTION OF DRAWINGS

**[0055] FIG. 1** presents a flow diagram of an example cyclic method for depositing and developing a photoresist in accordance with certain disclosed embodiments.

**[0056] FIG. 2** illustrates a pulse sequence for a hydrogen bromide (HBr) etchant and a chlorine ($Cl_2$) oxidizing agent for developing a photoresist in accordance with certain disclosed embodiments.

**[0057] FIG. 3A** shows a graph of chlorine oxidizing agent effect on residual byproduct thickness as temperature is varied in accordance with certain disclosed embodiments.

**[0058] FIG. 3B** shows a graph of hydrogen bromide etchant effect on residual byproduct thickness as the total exposure time of etchant is fixed but the etchant pulse duration of each cycle is varied in accordance with certain disclosed embodiments.

**[0059] FIG. 3C** shows a graph of chlorine oxidizing agent effect on residual byproduct thickness as oxidizing agent pulse duration is varied in accordance with certain disclosed embodiments.

**[0060] FIG. 4** shows scanning electron microscopy (SEM) images of a photopatterned substrate subjected to dry development with an etchant (single DD) in comparison to a photopatterned substrate subjected to cyclic dry development with etchant and chlorine oxidizing agent (cyclic DD) in accordance with certain disclosed embodiments.

**[0061] FIG. 5** shows a graphical comparison of the dry development with an etchant (single DD) in comparison to cyclic dry development with etchant and air oxidizing agent (cyclic DD) in accordance with certain disclosed embodiments.

**[0062] FIG. 6** presents a flow diagram of an example method for depositing and developing a photoresist utilizing an etchant in conjunction with a wash agent in accordance with certain disclosed embodiments.

**[0063] FIG. 7** depicts a schematic illustration of an example process station for maintaining a low-pressure environment that is suitable for performing the methods in accordance with certain disclosed embodiments.

**[0064] FIG. 8** depicts a schematic illustration of an example multi-station processing tool suitable for implementation of various operations in accordance with certain disclosed embodiments.

**[0071]** As used herein, the terms “top,” “bottom,” “upper,” “lower,” “above,” and “below” are used to provide a relative relationship between structures. The use of these terms does not indicate or require that a particular structure must be located at a particular location in the apparatus.

**[0072]** As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A OR B OR C), using a non-exclusive logical OR, and should not be construed to mean ‘at least one of A, at least one of B, and at least one of C.

**[0073]** By “atomic layer deposition” (ALD) is meant a vapor deposition process in which deposition cycles, preferably a plurality of consecutive deposition cycles, are conducted in a process chamber (i.e., a deposition chamber). Typically, during each cycle, the precursor is chemisorbed to a deposition surface (i.e., a substrate assembly surface or a previously deposited underlying surface such as material from a previous ALD cycle) forming a monolayer or sub-monolayer that does not readily react with additional precursor (i.e., a self-limiting reaction). Thereafter, if necessary, a reactant (i.e., another precursor or reaction gas) may be introduced into the process chamber for use in converting the chemisorbed precursor to the desired material on the deposition surface. Typically, this reactant is capable of reaction with the already chemisorbed precursor. Further, purging steps may also utilized during each cycle to remove excess precursor from the process chamber and/or remove excess reactant and/or reaction by-products from the process chamber after conversion of the chemisorbed precursor.

**[0074]** By “deposition” or “vapor deposition” is meant a process in which a metal layer is formed on one or more surfaces of a substrate from vaporized precursor composition(s) including one or more metal containing compounds. The metal-containing compounds are vaporized and directed to and/or contacted with one or more surfaces of a substrate (i.e., semiconductor substrate or semiconductor assembly) placed in a deposition chamber. Typically, the substrate is heated. These metal containing compounds form a non-volatile, thin, uniform metal-containing layer on the surface(s) of the substrate. One operation of the method is one cycle, and the process can be repeated for as many cycles necessary to obtain the desired metal thickness.

**[0075]** By “etchant” is meant any compound used to remove a material such as a layer, byproduct or contaminant from a surface.

**[0076]** By “wafer is meant a material which may include a substrate and a substrate layer to be etched. In some embodiments, the substrate layer includes an ashable hard mask such as spin-on carbon (SoC) or other material, e.g., silicon, silicon oxide, silicon nitride, silicon carbide, etc. In some embodiments, the substrate layer may be a layer stack disposed on the substrate.

such as HBr or HCl, as described in disclosed embodiments. In some embodiments, the heater 710 of the pedestal 708 may include a plurality of independently controllable temperature control zones.

**[0186]** Further, in some embodiments, pressure control for process station 700 may be provided by a butterfly valve 718. As shown in the embodiment of **FIG. 7**, butterfly valve 718 throttles a vacuum provided by a downstream vacuum pump (not shown). However, in some embodiments, pressure control of process station 700 may also be adjusted by varying a flow rate of one or more gases introduced to the process station 700.

**[0187]** In some embodiments, a position of showerhead 706 may be adjusted relative to pedestal 708 to vary a volume between the substrate 712 and the showerhead 706. Further, it will be appreciated that a vertical position of pedestal 708 and/or showerhead 706 may be varied by any suitable mechanism within the scope of the present disclosure. In some embodiments, pedestal 708 may include a rotational axis for rotating an orientation of substrate 712. It will be appreciated that, in some embodiments, one or more of these example adjustments may be performed programmatically by one or more suitable computer controllers 750.

**[0188]** Where plasma may be used, for example in gentle plasma-based dry development embodiments and/or etch operations conducted in the same chamber, showerhead 706 and pedestal 708 electrically communicate with a radio frequency (RF) power supply 714 and matching network 716 for powering a plasma. In some embodiments, the plasma energy may be controlled by controlling one or more of a process station pressure, a gas concentration, an RF source power, an RF source frequency, and a plasma power pulse timing. For example, RF power supply 714 and matching network 716 may be operated at any suitable power to form a plasma having a desired composition of radical species. Examples of suitable powers are up to about 500W.

**[0189]** In some embodiments, instructions for a controller 750 may be provided via input/output control (IOC) sequencing instructions. In one example, the instructions for setting conditions for a process phase may be included in a corresponding recipe phase of a process recipe. In some cases, process recipe phases may be sequentially arranged, so that all instructions for a process phase are executed concurrently with that process phase. In some embodiments, instructions for setting one or more reactor parameters may be included in a recipe phase. For example, a recipe phase may include instructions for setting a flow rate of a dry development chemistry reactant gas, such as HBr or HCl, and time delay instructions for

process chamber 924. Either or both of Faraday shield 949 and optional grid 950 may serve as a showerhead for delivery of process gases. In some embodiments, a liquid vaporization and delivery system may be situated upstream of the process chamber 924, such that once a liquid reactant or precursor is vaporized, the vaporized reactant or precursor is introduced into the process chamber 924 via a gas flow inlet 960 and/or 970.

**[0216]** Radio frequency power is supplied from the RF power supply 941 to the coil 933 to cause an RF current to flow through the coil 933. The RF current flowing through the coil 933 generates an electromagnetic field about the coil 933. The electromagnetic field generates an inductive current within the upper sub-chamber 902. The physical and chemical interactions of various generated ions and radicals with the wafer 919 etch features of and selectively deposit layers on the wafer 919.

**[0217]** If the plasma grid 950 is used such that there is both an upper sub-chamber 902 and a lower sub-chamber 903, the inductive current acts on the gas present in the upper sub-chamber 902 to generate an electron-ion plasma in the upper sub-chamber 902. The optional internal plasma grid 950 limits the amount of hot electrons in the lower sub-chamber 903. In some embodiments, the apparatus 900 is designed and operated such that the plasma present in the lower sub-chamber 903 is an ion-ion plasma.

**[0218]** Both the upper electron-ion plasma and the lower ion-ion plasma may contain positive and negative ions, though the ion-ion plasma will have a greater ratio of negative ions to positive ions. Volatile etching and/or deposition byproducts may be removed from the lower sub-chamber 903 through port 922. The chuck 917 disclosed herein may operate at elevated temperatures ranging between about 10°C and about 250°C. The temperature will depend on the process operation and specific recipe.

**[0219]** Apparatus 900 may be coupled to facilities (not shown) when installed in a clean room or a fabrication facility. Facilities include plumbing that provide processing gases, vacuum, temperature control, and environmental particle control. These facilities are coupled to apparatus 900, when installed in the target fabrication facility. Additionally, apparatus 900 may be coupled to a transfer chamber that allows robotics to transfer semiconductor wafers into and out of apparatus 900 using typical automation.

**[0220]** In some embodiments, a system controller 930 (which may include one or more physical or logical controllers) controls some or all of the operations of a process chamber 924. The system controller 930 may include one or more memory devices and one or more processors. In some embodiments, the apparatus 900 includes a switching system for controlling flow rates and durations when disclosed embodiments are performed. In some

moved into and out of for deposition and etching as described herein. Or, as described below, the EUVL patterning tool may be a module on a larger multi-component tool. **FIG. 10** depicts a semiconductor process cluster tool architecture with vacuum-integrated deposition, EUV patterning and dry development/etch modules that interface with a vacuum transfer module, suitable for implementation of the processes described herein. While the processes may be conducted without such vacuum integrated apparatus, such apparatus may be advantageous in some embodiments.

**[0227] FIG. 10** depicts a semiconductor process cluster tool architecture 1000 with vacuum-integrated deposition and patterning modules that interface with a vacuum transfer module, suitable for implementation of processes described herein. The arrangement of transfer modules to "transfer" wafers among multiple storage facilities and processing modules may be referred to as a "cluster tool architecture" system. Deposition and patterning modules are vacuum-integrated, in accordance with the requirements of a particular process. Other modules, such as for etch, may also be included on the cluster.

**[0228]** A vacuum transport module (VTM) 1038 interfaces with four processing modules 1020a–1020d, which may be individually optimized to perform various fabrication processes. By way of example, processing modules 1020a–1020d may be implemented to perform deposition, evaporation, ELD, dry development, etch, strip, and/or other semiconductor processes. For example, module 1020a may be an ALD reactor that may be operated to perform in a non-plasma, thermal atomic layer depositions as described herein. It should be understood that the figure is not necessarily drawn to scale.

**[0229]** Airlocks 1042 and 1046, also known as a loadlocks or transfer modules, interface with the VTM 1038 and a patterning module 1040. This tool architecture allows for work pieces, such as semiconductor substrates or wafers, to be transferred under vacuum so as not to react before exposure. Integration of the deposition modules with the lithography tool is facilitated by the fact that EUVL also requires a greatly reduced pressure given the strong optical absorption of the incident photons by ambient gases such as $H_2O$, $O_2$, etc.

**[0230]** As noted above, this integrated architecture is just one possible embodiment of a tool for implementation of the described processes. The processes may also be implemented with a more conventional stand-alone EUVL scanner and a deposition reactor, either stand alone or integrated in a cluster architecture with other tools, such as etch, strip etc., as modules, for example as described with reference to **FIG. 10** but without the integrated patterning module.

**[0231]** Airlock 1042 may be an "outgoing" loadlock, referring to the transfer of a substrate out from the VTM 1038 serving a deposition module 1020a to the patterning module 1040, and