CLAIMS

1. A manufacturing method of a semiconductor structure, comprising:

providing a substrate, a plurality of spaced first trenches being formed in the substrate, and the first trenches extending along a first direction;

forming a sacrificial layer in the first trenches and a first protective layer on the sacrificial layer, the sacrificial layer and the first protective layer filling up the first trenches, and the first protective layer in the first trenches being provided with etching holes penetrating through the first protective layer;

removing the sacrificial layer located under the etching holes to form air gaps; and

carrying out a silicidation reaction on the substrate between adjacent ones of the first trenches and close to bottoms of the first trenches, so as to form, in the substrate, bit lines (BLs) extending along the first direction, parts of side surfaces of the BLs being exposed in the air gaps;

wherein the carrying out a silicidation reaction on the substrate between adjacent ones of the first trenches and close to bottoms of the first trenches, so as to form, in the substrate, BLs extending along the first direction, parts of side surfaces of the BLs being exposed in the air gaps comprises:

etching the substrate and the first protective layer to form a plurality of spaced second trenches, the second trenches extending along a second direction and not communicating with the air gaps;

forming a second protective layer on sidewalls of the second trenches, the second protective layer in the second trenches enclosing third trenches; and

depositing metal on bottoms of the third trenches, and carrying out the silicidation reaction by annealing to form the BLs.

2. The manufacturing method of a semiconductor structure according to claim 1, wherein the forming a sacrificial layer in the first trenches and a first protective layer on the sacrificial layer, the sacrificial layer and the first protective layer filling up the first trenches, and the first protective layer in the first trenches being provided with etching holes penetrating through the first protective layer comprises:

depositing the sacrificial layer in the first trenches, the sacrificial layer filling the bottoms of the first trenches;

depositing the first protective layer on the sacrificial layer, the first protective layer leveling off the first trenches; and

etching the first protective layer at edges of the first trenches to form the etching holes.

3. The manufacturing method of a semiconductor structure according to claim 2, wherein the depositing the first protective layer on the sacrificial layer, the first protective layer leveling off the first trenches comprises:

depositing the first protective layer on the sacrificial layer and the substrate, the first protective layer filling the first trenches and covering a top surface of the substrate; and

removing the first protective layer on the top surface of the substrate to expose the substrate.

4. The manufacturing method of a semiconductor structure according to claim 1, wherein the etching holes extend to the sacrificial layer.

5. The manufacturing method of a semiconductor structure according to claim 1, wherein a material of the BLs comprises metal silicide.

6. The manufacturing method of a semiconductor structure according to claim 1, before the etching the substrate and the first protective layer to form a plurality of spaced second trenches, the second trenches extending along a second direction and not communicating with the air gaps, the manufacturing method further comprises:

depositing a third protective layer on the substrate and the first protective layer; and

the etching the substrate and the first protective layer to form a plurality of spaced second trenches comprises: etching the substrate, the first protective layer and the third protective layer to form the plurality of spaced second trenches, and remaining the third protective layer between adjacent ones of the second trenches.

7. The manufacturing method of a semiconductor structure according to claim 6, wherein the forming a second protective layer on sidewalls of the second trenches, the

second protective layer in the second trenches enclosing third trenches comprises:

depositing a second initial protective layer on the sidewalls and bottoms of the second trenches and on the third protective layer; and

etching the second initial protective layer on the third protective layer and on the bottoms of the second trenches to expose the bottoms of the second trenches, the remaining second initial protective layer forming the second protective layer.

8. The manufacturing method of a semiconductor structure according to claim 6, wherein the first protective layer, the second protective layer and the third protective layer are made of a same material.

9. The manufacturing method of a semiconductor structure according to claim 1, before the forming a second protective layer on sidewalls of the second trenches, the second protective layer in the second trenches enclosing third trenches, the manufacturing method further comprises:

forming active regions in the substrate away from the bottoms of the first trenches, wherein the active regions each comprise a source region, a drain region and a channel region; and the source region, the channel region and the drain region are arranged sequentially along a direction perpendicular to the bottoms of the first trenches.

10. The manufacturing method of a semiconductor structure according to claim 9, after the depositing metal on bottoms of the third trenches, and carrying out the silicidation reaction by annealing to form the BLs, the manufacturing method further comprises:

forming first insulating layers in the third trenches, the first insulating layers filling the third trenches;

removing, along a direction perpendicular to the substrate, the first protective layer and the second protective layer to a preset depth to form filling spaces, the filling spaces exposing side surfaces of the active regions; and

forming gate structures in the filling spaces, the gate structures extending along the second direction and surrounding the active regions.

11. The manufacturing method of a semiconductor structure according to claim 10, wherein the first protective layer and the first insulating layers are made of different

materials.

12. The manufacturing method of a semiconductor structure according to claim 10, wherein the removing, along a direction perpendicular to the substrate, the first protective layer and the second protective layer to a preset depth to form filling spaces, the filling spaces exposing side surfaces of the active regions comprises:

etching the second protective layer and the first protective layer to an initial depth to form filling channels;

depositing a second insulating layer in the filling channels, the second insulating layer filling up the filling channels between the substrate and the first insulating layers; and

etching the remaining first protective layer and the remaining second protective layer to the preset depth to form the filling spaces.

13. The manufacturing method of a semiconductor structure according to claim 10, wherein the forming gate structures in the filling spaces, the gate structures extending along the second direction and surrounding the active regions comprises:

forming oxide layers on inner surfaces of the filling spaces; and

forming conductive layers in the filling spaces after the oxide layers are formed, the conductive layers being opposite to at least parts of the channel regions.

14. The manufacturing method of a semiconductor structure according to claim 12, after the forming gate structures in the filling spaces, the gate structures extending along the second direction and surrounding the active regions, the manufacturing method further comprises:

depositing a third insulating layer on the gate structures, the third insulating layer covering the gate structures and fulling up the remaining filling channels.

15. The manufacturing method of a semiconductor structure according to claim 14, wherein the first insulating layers, the second insulating layer and the third insulating layer are made of a same material.

16. A semiconductor structure, comprising:

a substrate, wherein a plurality of spaced bit lines (BLs) are formed in the substrate, the BLs extend along a first direction, first trenches are formed between adjacent two

of the BLs, the BLs each are provided thereon with at least an active region, the active region comprises a source region, a channel region and a drain region that are stacked sequentially, and one of the source region and the drain region is electrically connected to the BL;

a protective layer in the first trenches, wherein air gaps are formed between the protective layer and bottoms of the first trenches, and parts of side surfaces of the BLs are exposed in the air gaps;

a plurality of spaced first insulating layers on the protective layer, wherein the first insulating layers extend along a second direction, and the first insulating layers are located between adjacent two rows of the active regions in the second direction, and spaced apart from the active regions;

gate structures between the first insulating layers and the active regions, wherein the gate structures extend along the second direction and surround the active regions, and the gate structures are opposite to at least parts of the channel regions; and

a second insulating layer and a third insulating layer covering the gate structures.

17. The semiconductor structure according to claim 16, the semiconductor structure further comprises:

a contact node on the other of the source region and the drain region, and a capacitor on the contact node.