Claims

1. An apparatus for synchronization by determining a clock offset between a current receiver clock time and a correct receiver clock time, wherein the apparatus comprises:

an input interface for receiving information on a received synchronization sequence comprising a sequence of symbols, wherein the information on the received synchronization sequence comprises information for each symbol of a plurality of symbols of the sequence of symbols that said symbol exhibits a first state out of two or more possible states being different from a second state of the two possible states; and

an offset analyser for determining the clock offset by determining an analysis result for each of a plurality of levels depending on the received synchronization sequence and depending on a level pattern being associated with said level, and by determining the clock offset using the analysis result of each of the plurality of levels, wherein the level pattern for each of the plurality of levels comprises a sequence of symbols and is different from any other level pattern of the plurality of levels.

2. An apparatus according to claim 1,

wherein the input interface is configured to receive the received synchronization sequence from another apparatus, and

wherein, for the synchronization, the apparatus is configured to not transmit any message to said other apparatus.

3. An apparatus according to claim 1 or 2,

wherein each symbol of the sequence of symbols of the synchronization sequence is randomly or pseudo-randomly associated with a level out of the plurality of levels such that the state of said symbol of the sequence of symbols corresponds to a state of a symbol of the level pattern being associated with said level.

4. An apparatus according to one of the preceding claims,

wherein the synchronization sequence that is received as the received synchronization sequence has been generated such that the synchronization sequence comprises symbols of the level pattern of each level of the plurality of levels, wherein each symbol of the symbols of said level pattern is encoded by the state of one or more symbols of the sequence of symbols of the synchronization sequence,

wherein the synchronization sequence has been generated such that for each symbol position in the synchronization sequence, the level pattern of one of the plurality of levels has been chosen for determining a symbol for said symbol position in the synchronization sequence, such that the symbols of different level patterns are mixed within the synchronization sequence, such that the synchronization sequence does not comprise the symbols of a level pattern of one of the plurality of levels in a correct order.

5. An apparatus according to one of the preceding claims,

wherein a first one of the symbols of the synchronization sequence exhibits a state that corresponds to the state of a symbol of the level pattern being associated with a first level out of the plurality of levels,

wherein a second one of the symbols of the synchronization sequence, which immediately succeeds the first one of the symbols within the synchronization sequence, exhibits a state that corresponds to the state of a symbol of the level pattern being associated with a second level out of the plurality of levels, the second level being different from the first level, and

wherein a third one of the symbols of the synchronization sequence, which immediately succeeds the second one of the symbols within the synchronization sequence, exhibits a state that corresponds to the state of a symbol of the level pattern being associated with a third level out of the plurality of levels, the third level being different from the second level.

6. An apparatus according to claim 1 or 2,

wherein the synchronization sequence that is received as the received synchronization sequence has been generated such that it comprises one or more

occurrences of the level pattern of each level of the plurality of levels in a correct order.

7. An apparatus according to one of the preceding claims,

wherein the offset analyser is configured to determine the analysis result for each level ℓ of the plurality of levels by determining for said level, whether or not the offset exhibits at least $2^{\ell-1}$ time units, wherein a time unit is equal to a duration of a symbol of the sequence of symbols, or is equal to a positive multiple m of the duration of a symbol of the sequence of symbols, wherein the level ℓ is an integer value with $\ell \geq 0$ for each of the plurality of levels, wherein m is a real value with $m > 0$.

8. An apparatus according to claim 7,

wherein the offset analyser is configured to determine a level offset for each level ℓ of the plurality of levels, such that the level offset for said level ℓ is either $2^{\ell-1}$ time units or is 0;

wherein the clock offset corresponds to a sum of the level offset of each level ℓ of the plurality of levels, or corresponds to a difference of the sum and $2^{\ell_{\max}}$, or corresponds to an integer multiple of said sum or of said difference, or corresponds to said sum or of said difference divided by a predefined value.

9. An apparatus according to claim 8,

wherein the offset analyser is configured to determine for each level of the plurality of levels and a comparison result for each symbol of at least a portion of the plurality of symbols, which exhibits the first state, whether a symbol at a corresponding position in the level pattern of the said level exhibits the first state or exhibits the second state,

wherein the offset analyser is configured to determine the level offset such that the level offset is 0, if for said level more comparison results have been determined where the compared symbols exhibit a same state compared to comparison results for said level where the compared symbols exhibit a different state, and

wherein the offset analyser is configured to determine the level offset such that the level offset exhibits $2^{\ell-1}$ time units, if for said level more comparison results or a

same number of comparison results have been determined where the compared symbols exhibit a different state compared to comparison results for said level where the compared symbols exhibit the same state.

10. An apparatus according to claim 9,

wherein the level offset for each level is determined subsequently starting from a smallest level among the plurality of levels.

11. An apparatus according to claim 10,

wherein, if the offset analyser has determined for a level of the plurality of levels that a level offset exhibits $2^{\ell-1}$ time units, the plurality of symbols of the received synchronization sequence are shifted by the level offset for said level before determining the level offset for a subsequent level of the plurality of levels.

12. An apparatus for generating a synchronization sequence for synchronization, wherein the apparatus comprises:

a synchronization sequence generator for generating, using a plurality of level patterns, the synchronization sequence comprising a sequence of symbols, and

an output interface for outputting or transmitting the synchronization sequence,

wherein the level pattern of each of the plurality of level patterns comprises a sequence of symbols, wherein each of the plurality of symbols of each of the plurality of level patterns exhibits a state out of two or more possible states, wherein the level pattern of each of the plurality of level patterns is different from any other level pattern of the plurality of level pattern,

wherein the synchronization sequence generator is configured to generate the synchronization sequence by assigning, to each symbol of the sequence of symbols of the synchronization sequence, the state of one of the plurality of symbols of one of the plurality of level patterns.

13. An apparatus according to claim 12,

wherein the apparatus is configured to transmit the synchronization sequence to a further apparatus, and

wherein, for the synchronization, the apparatus is configured to not receive any message from said further apparatus.

14. An apparatus according to claim 12 or 13,

wherein the synchronization sequence generator is configured to select, for each symbol of the sequence of symbols of the synchronization sequence, a level out of the plurality of levels, and

wherein the synchronization sequence generator is configured to assign a symbol of the plurality of symbols of the level pattern associated with said level to said symbol of the sequence of symbols of the synchronization sequence.

15. An apparatus according to claim 14,

wherein the synchronization sequence generator is configured to select, for each symbol of the sequence of symbols of the synchronization sequence, the level out of the plurality of levels, randomly or pseudo-randomly.

16. An apparatus according to one of claims 12 to 15,

wherein the synchronization sequence generator is configured to generate the synchronization sequence such that the synchronization sequence comprises symbols of the level pattern of each level of the plurality of levels,

wherein the synchronization sequence generator is configured to generate the synchronization sequence such that for each symbol position in the synchronization sequence, the level pattern of one of the plurality of levels is chosen for determining a symbol for said symbol position in the synchronization sequence, such that the symbols of different level patterns are mixed within the synchronization sequence, such that the synchronization sequence does not comprise the symbols of a level pattern of one of the plurality of levels in a correct order.

17. An apparatus according to claim 12 or 13,

wherein each level out of the plurality of levels belongs to a group out of one or more groups,

wherein the synchronization sequence generator is configured to select, for a symbol of the sequence of symbols of the synchronization sequence, a level out of a current group out of the one or more groups, and

wherein the synchronization sequence generator is configured to assign a symbol of the plurality of symbols of the level pattern associated with said level to said symbol of the sequence of symbols of the synchronization sequence.

18. An apparatus according to claim 12 or 13,

wherein the synchronization sequence generator is configured to generate the synchronization sequence such that it comprises one or more occurrences of the level pattern of each level of the plurality of levels in a correct order.

19. An apparatus according to one of claims 12 to 18,

wherein the synchronization sequence generator is configured to assign a symbol of the plurality of symbols of the level pattern associated with a first level of out the plurality of levels to a first one of the symbols of the synchronization sequence,

wherein the synchronization sequence generator is configured to assign a symbol of the plurality of symbols of the level pattern associated with a second level of out the plurality of levels to a second one of the symbols of the synchronization sequence, the second one of the symbols of the synchronization sequence being an immediate successor of the first one of the symbols of the synchronization sequence, the second level being different from the first level, and

wherein the synchronization sequence generator is configured to assign a symbol of the plurality of symbols of the level pattern associated with a third level of out the plurality of levels to a third one of the symbols of the synchronization sequence, the third one of the symbols of the synchronization sequence being an immediate successor of the second one of the symbols of the synchronization sequence, the third level being different from the second level.

20. An apparatus according to one of claims 12 to 19,

wherein each symbol of the plurality of symbols of the level pattern of each level either exhibits a first bit value out of two possible bit values or a second bit value out of the two possible bit values,

wherein each of the plurality of symbols of said level pattern is encoded by a state of one or more symbols of the plurality of symbols of the level pattern,

wherein the synchronization sequence comprises a sequence of symbols, wherein each of the sequence of symbols of the synchronization sequence is encoded by a state of one or more symbols of the sequence of symbols of the synchronization sequence,

wherein the synchronization sequence generator is configured to generate the sequence of symbols of the synchronization sequence by assigning one of the plurality of symbols of the level pattern of a level as a symbol of the synchronization sequence for each of the sequence of symbols of the synchronization sequence.

21. An apparatus according to claim 20,

wherein the level pattern for each level ℓ of the plurality of levels comprises a first sequence of $c \times 2^{\ell-1}$ symbols which exhibit the first bit value, immediately followed by a second sequence of symbols which exhibit the second bit value; or wherein the level pattern for each level ℓ of the plurality of levels comprises the second sequence of $c \times 2^{\ell-1}$ symbols which exhibit the second bit value, immediately followed by the first sequence of $c \times 2^{\ell-1}$ symbols which exhibit the first bit value, wherein c is a real positive value.

22. A system comprising:

an apparatus according to one of claims 12 to 21 for generating a synchronization sequence for synchronization, and

an apparatus according to one of claims 1 to 11 for synchronization by determining a clock offset,

wherein the input interface of the apparatus for synchronization by determining the clock offset is configured to receive the received synchronization sequence, or a part

of it, being generated by the apparatus for generating the synchronization sequence, and

wherein the offset analyser of the apparatus for synchronization by determining the clock offset is configured to determine the clock offset by determining the analysis result for each of the plurality of levels depending on the received synchronization sequence and depending on the level pattern being associated with said level, and by determining the clock offset using the analysis result of each of the plurality of levels.

23. A system according to claim 22,

wherein the system comprises one or more further apparatuses according to one of claims 1 to 11 for synchronization by determining a clock offset,

wherein the input interface of each of the further apparatuses for synchronization by determining the clock offset is configured to receive the received synchronization sequence being generated by the apparatus for generating the synchronization sequence, and

wherein the offset analyser of each of the further apparatuses for synchronization by determining the clock offset is configured to determine the clock offset by determining the analysis result for each of the plurality of levels depending on the received synchronization sequence and depending on the level pattern being associated with said level, and by determining the clock offset using the analysis result of each of the plurality of levels.

24. A method for synchronization by determining a clock offset between a current receiver clock time and a correct receiver clock time, wherein the method comprises:

receiving information on a received synchronization sequence comprising a sequence of symbols, wherein the information on the received synchronization sequence comprises information for each symbol of a plurality of symbols of the sequence of symbols that said symbol exhibits a first state out of two or more possible states being different from a second state of the two possible states; and

determining the clock offset by determining an analysis result for each of a plurality of levels depending on the received synchronization sequence and depending on a

level pattern being associated with said level, and by determining the clock offset using the analysis result of each of the plurality of levels, wherein the level pattern for each of the plurality of levels comprises a sequence of symbols and is different from any other level pattern of the plurality of levels.

25. A method for generating a synchronization sequence for synchronization, wherein the method comprises:

generating, using a plurality of level patterns, the synchronization sequence comprising a sequence of symbols, and

outputting or transmitting the synchronization sequence,

wherein the level pattern of each of the plurality of level patterns comprises a sequence of symbols, wherein each of the plurality of symbols of each of the plurality of level patterns exhibits a state out of two or more possible states, wherein the level pattern of each of the plurality of level patterns is different from any other level pattern of the plurality of level pattern,

wherein generating the synchronization sequence comprises assigning, to each symbol of the sequence of symbols of the synchronization sequence, the state of one of the plurality of symbols of one of the plurality of level patterns.

26. A computer program for implementing the method of claim 24 or 25 when being executed on a computer or signal processor.